1963

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Monterey, California: U.S. Naval Postgraduate School

http://hdl.handle.net/10945/12494

INVESTIGATION OF TWO STAGE MAGNETIC AMPLIFIERS

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and
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Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING

United States Naval Postgraduate School
Monterey, California

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ABSTRACT

Two stage magnetic amplifiers are extensively used in many applications, but several types have not previously been mathematically analyzed. The Hybrid III is described in detail and analyzed by the method of finite difference equations. Experimental data confirms the analysis for negligible source resistance of the power supplies, but shows that the analysis is invalid for appreciable supply source resistance. Further examination reveals the cause of the strong effect of source resistance. The Hybrid IV is described in detail and analyzed by the same method. Experimental data fails to confirm the analysis completely, but when steps are taken to eliminate diode unblocking, the gain is confirmed.

The authors wish to express their appreciation for the assistance in conception and development of the analysis rendered by Mr. Raymond B. Yarbrough of the U. S. Naval Postgraduate School.

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INTRODUCTION

Magnetic amplifiers have been in use for many years, and have become more in demand recently for military and space applications where a high degree of reliability and relative insensitivity to environmental conditions are desired. Although many analyses of specific magnetic amplifier circuits have been made in recent years, there are still several classes of circuits which are being designed and built only on the basis of laboratory experiment and personal experience. In particular, Lynn, Pula, Ringleman and Timmel (1) state that the transfer function of the type of circuit known as Hybrids "have not been very thoroughly investigated, other than experimentally." In particular, they state that if the Hybrid III circuit did not have the advantages of high gain and fast response, it would probably not be considered practical, because of analytical problems associated with the interstage circuit which couples the first stage gate and second stage signal windings.

Johannessen (2) has provided a method of analysis of magnetic amplifiers by the use of difference equations. It is the purpose of this paper to apply this method to the Hybrid III and IV circuits, in the hope that a successful analysis will lead to future design of these circuits by analytical, rather than experimental, methods.

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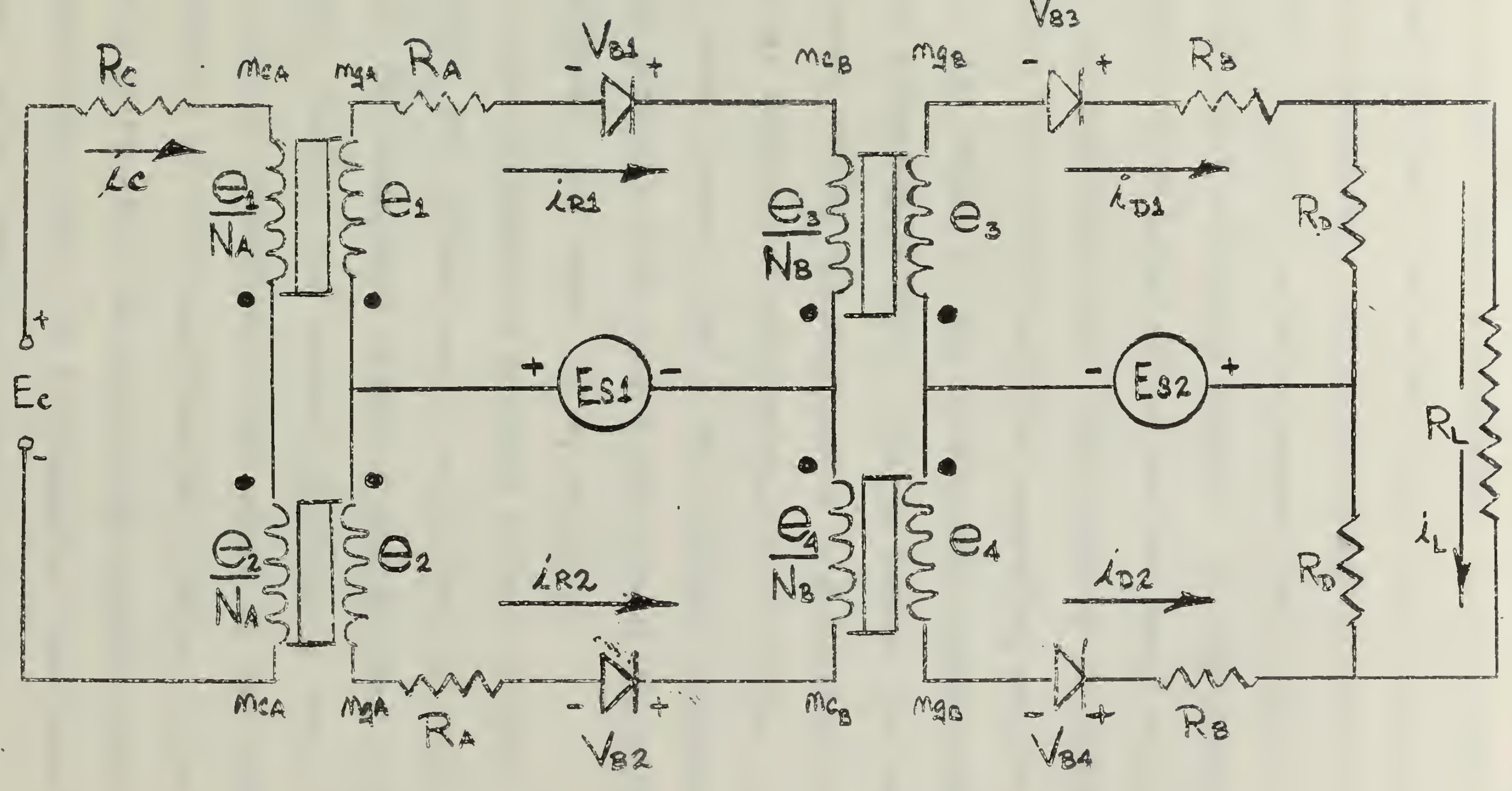
II

THE HYBRID III AMPLIFIER

A. Introduction and Description

The Hybrid III magnetic amplifier circuit is shown in Fig. 1. This circuit is a two stage amplifier with push-pull output. It has the advantages of high gain and fast response, with a basic one cycle time delay. This circuit will accept a phase reversible a.c. or polarity reversible d.c. input, with a resulting polarity reversible average d.c. output. Because of the half cycle output of the circuit and its one cycle time delay, feedback may be employed directly. This is not true in the single stage amplifier of this type, because with only a half cycle output, and a half cycle time delay, a portion of the output fed back to the input core will arrive there during the gating half cycle, when input has no effect on the average output. With such a two stage amplifier as the Hybrid III, the output from the second stage occurs during the reset half cycle of the first stage, making feedback realizable.

A brief description of the circuit's operation follows. The diodes are so arranged that, barring diode unblocking, the input cores can receive gating voltage only from the coupling loop source voltage. Therefore, in the absence of input voltage, cores 1 and 2 will receive no reset and remain saturated. The core sized and turns ratios are arranged so that the current flowing in the coupling loop prior to input core saturation is insufficient to cause



THE HYBRID III MAGNETIC AMPLIFIER CIRCUIT

FIGURE 1

[illegible]

resetting of the output cores. Therefore, because of the output circuit diode arrangement, if the input core remains unsaturated, the output core will receive no reset, and remain unsaturated. (Gating voltage is provided by the output source voltage in the alternate half cycle to that in which the input cores are gated.) In the absence of an input voltage, both input cores are saturated by the voltage source in the coupling loop. This results in currents in both coupling loops which provide resetting mmf for the output cores. The ratio of the output and coupling loop source voltages is adjusted so that, with no input, the output cores gate and reset during alternate half cycles, just reaching saturation at the end of each gating half cycle. In this condition, since cores 3 and 4 are matched, whatever small magnetizing currents flow in the two output loops are exactly balanced, and there is no output.

If an input voltage is applied to the circuit, it provides reset for either core 1 or 2, but not both. This results in incomplete reset of either core 3 or core 4, but not both, because the current flowing in one of the coupling loops is insufficient for reset of the output core during a portion of its resetting half cycle. This in turn leads to saturation of one of the output cores during the following half cycle, an accompanying unbalance of the output loops, and a resulting output current.

There is a phenomenon occurring in the output cores of this circuit which was not realized in the early stages

of the analysis. That is, because of the configuration of the output circuit, there is in the unsaturated output core (whose reset voltage has not been effected by input voltage), a reduction of gating voltage during the portion of the half cycle when output current is flowing. Since the voltages are adjusted so that with no input there is complete reset of the output cores, this reduction in gating voltage leads to negative saturation of this core during the next half cycle. At first glance this situation seems to provide no problem, since current in this half cycle is blocked by the output diode. However, it will be shown later in the analysis that if there is any source resistance in the coupling loop supply voltage, this negative saturation of an output core will result in a nonlinear positive feedback effect, which in turn results in a departure from the one cycle response time.

B. Outline of the analysis.

1. Procedure.

The procedure used in this magnetic amplifier analysis is summarized as follows.

a. The circuit and cores were examined qualitatively to determine the modes of operation that were of interest, assuming that the circuit and cores operated linearly within each of this modes.

b. Loop equations for each loop of the circuit, and mode equations relating core voltage and current for each core of the circuit were written for each mode. These

equations were solved separately for each mode, to obtain the core voltages and currents of interest.

c. Applying the principle of Faraday's law that the volt-time integral (change of flux) over a full cycle must equal zero for any core which is cycling in a steady state, the volt-second equation was written for each core. These equations reduced to expressions in terms of the core voltages in individual modes that had already been solved for, and core firing times.

d. The expression for the half cycle average value of load current in terms of mode solutions for load current and core firing times was found. Core firing times were solved for.

e. The value of core firing times in terms of circuit parameters and output current, plus the values of core voltages in terms of circuit parameters and input voltage were substituted into the previously written volt-second equations. Rearrangement of these equations gave an expression for output in a given half cycle in terms of circuit parameters and input in one or mode previous half cycles. This expression, the output difference equation, describes the operation of the circuit. Its limits were found from re-examination of each mode, and when these were determined, the difference equation provided the circuit's transfer characteristic. This transfer characteristic, and the circuit's time delay, provide all necessary information for design.

C. The Analysis.

1. Assumptions. The circuit used in this analysis has been shown in Fig. 1. Definitions of parameters are given in Fig. 2. It was originally assumed that:

a. The first stage cores are identical, as are the second stage cores. The hysteresis loop of each core is "square", and the unsaturated core function is as follows:

$$\sum_{i} n_i \, i_i = \pm n_g \, I_o + n_g \, G \, e$$

that is, the sum of all ampere turns applied to the core is equal to the static magnetizing mmf plus a constant times the voltage appearing at the gate winding, accounting for eddy currents. The plus and minus sign are to provide applicability to both the gating and resetting situations. The method for determining the constants is described in Appendix A.

b. Before core 1 reaches saturation, its gating current is less than the static magnetizing current of core 3. Therefore, this current is insufficient to change the condition of flux in core 3. Before core 2 saturates, its gating current is likewise insufficient to effect core 4.

c. The source voltages are square waves, in phase, with negligible source resistance.

d. The input voltage is a constant, or varies slowly enough with respect to the source voltages to be considered a constant during a half cycle of source voltage.

Fig. 2. - Nomenclature

e_1, e_2, e_3, e_4 = instantaneous core voltage, output winding

e_{s1}, e_{s2} = instantaneous value of supply voltages

e_c = instantaneous value of control voltage

$E_{c(n)}$ = control voltage assumed constant over a given half cycle

E_{s1}, E_{s2} = magnitude of square wave supply voltage

G = dynamic core conductance, equal to the ratio between change in loop width and core voltage

i = instantaneous current

$I_{(n)}$ = average current, averaged over a specified half cycle of supply voltage

I_o = magnetizing current corresponding to the static core loop width, referred to the output winding

K_1, K_2, K_3, = derived constants in difference equation

$n-1$, n, $n+1$ = three consecutive half cycles of the supply voltage

N_A, N_B = turns ratio of the output winding to the control winding, of input (A), and output (B) cores

R_A = resistance of coupling circuit, including windings and forward resistance of diodes

R_B = resistance of output circuit, not including dividing or load resistance

R_{s1},R_{s2} = source resistance

R_c = resistance of control circuit including windings and source resistance

R_D = dividing resistance

R_L = load resistance

T = period of one half cycle of supply voltage

V_b = back voltage on a diode when not conducting

$\alpha(n)$ = time, measured from beginning of half cycle, when input core saturates

$\beta(n)$ = time, measured from beginning of half cycle, when output core saturates

DEFINITION OF TERMS

Gating = The change of flux toward positive saturation.

Resetting = The change of flux away from positive saturation.

Gating-Half Cycle = The half cycle in which a core normally gates.

Reset-Half Cycle = The half cycle in which a core normally is reset.

Firing time = The instant of saturation of a core.

Diode Blocking = The diode is reverse biased.

Diode Un-Blocking = The diode is forward biased during a half cycle when it is normally blocked.

e. Diode unblocking does not occur. That is, when the source voltage is of such polarity as to oppose current flow through a diode, it is assumed that the combination of core voltages in the loop is insufficient to overcome this source voltage and cause current to flow. In situations where this is not the case, it will be shown later, a special non-symmetrical source voltage can be devised which will force the the assumption to be true.

2. Assumed Modes of Operation. A preliminary examination of the operation of the circuit revealed that there are four modes of operation, and that with the assumptions made, the circuit's operation is linear within each mode. The polarity of output voltage will depend on that of the input voltage. With the polarity of input voltage as shown in Fig. 1., the modes are as follows:

Mode I. Assume that at t=0, core 1 is at some intermediate flux level, cores 2 and 3 are saturated, and core 4 has just reached saturation. The source voltages have just reversed to positive polarity as marked. During this mode:

Core 1 is gating
Core 2 remains saturated
Core 3 remains saturated
Core 4 is resetting

This condition continues until core 1 saturates.

Mode II. Source voltage polarities remain as in Mode I.

Core 1 is saturated

Core 2 is saturated

Core 3 is resetting

Core 4 is resetting

This condition continues until the source voltages reverse polarity.

Mode III. In this mode:

Core 1 is resetting

Core 2 is saturated

Core 3 is gating

Core 4 is gating

This mode continues until core 3 saturates.

Mode IV. In this mode:

Core 1 is resetting

Core 2 is saturated

Core 3 is saturated

Core 4 is gating

Because of the symmetry of the circuit, the operation will be the same with the input voltage polarity reversed, provided that the core numbers 1 and 2 are interchanged as are core numbers 3 and 4, in the above description.

Certain characteristics of the circuit's operation became evident from the above. First, load current could only flow in Mode IV. Second, with the input polarity

as shown, core 2 never comes out of saturation. Thus it was assumed that core 4 would alternate between gating for one half cycle and resetting the next, provided that the values of the source voltages and circuit resistances were appropriate. The values necessary for this condition will be developed in the analysis. It will also be shown that under certain conditions, part of this hypothesis was not valid.

3. Statement of Modal Equations. Using the preceding section as a guide, the equations for each mode were written as follows: (Note that source voltage polarities are not inserted here.)

Mode I:

The following variables are zero in this mode:

e_2, e_3, V_{b1}, V_{b2}, i_{D1}, i_{D2}, i_L.

$$e_c = i_c R_c - e_1/N_A$$

$$e_{s1} = e_1 + i_{R1} R_A$$

$$e_{s1} = i_{R2} R_A - e_4/N_B$$

$$-e_{s2} = -V_{b3}$$

$$-e_{s2} = e_4 - V_{b4}$$

$$-i_c/N_A + i_{R_1} = I_{oA} + G_A e_1$$

$$-i_{R2}/N_B = -I_{oB} + G_B e_4$$

Mode II:

The following variables are zero in this mode:

e_1, e_2, V_{b1}, V_{b2}, i_{D1}, i_{D2}, i_L

$$e_c = i_c R_c$$

$$e_{s1} = i_{R1} R_A - e_3/N_B$$

$$e_{S1} = i_{R2} R_A - e_4/N_B$$

$$-e_{S2} = e_3 - V_{b3}$$

$$-e_{S2} = e_4 - V_{b4}$$

$$-i_{R1}/N_B = -I_{oB} + G_B e_3$$

$$-i_{R2}/N_B = -I_{oB} + G_B e_4$$

Mode III:

The following variables are zero in this mode:

i_{R1}, i_{R2}, e_2, V_{b3}, V_{b4}

$$e_c = i_c R_c - e_1/N_A$$

$$e_{S1} = e_1 - e_3/N_B - V_{b1}$$

$$e_{S1} = -e_4/N_B - V_{b2}$$

$$-e_{S2} = e_3 + i_{D1} (R_B + R_D) - i_L R_D$$

$$-e_{S2} = e_4 + i_{D2} (R_B + R_D) + i_L R_D$$

$$-i_c/N_A = -I_{oA} + G_A e_1$$

$$i_{D1} = I_{oB} + G_B e_3$$

$$i_{D2} = I_{oB} + G_B e_4$$

$$i_L(2R_D+R_L) + i_{D2} R_D - i_{D1} R_D = 0$$

Mode IV:

The following variables are zero in this mode:

e_2, e_3, i_{R1}, i_{R2}, V_{b3}, V_{b4}.

$$e_c = i_c R_c - e_1/N_A$$

$$e_{S1} = e_1 - V_{b1}$$

$$e_{S1} = -e_4/N_B - V_{b2}$$

$$-e_{S2} = i_{D1}(R_B + R_D) - i_L R_D$$

$$-e_{S2} = e_4 + i_{D2}(R_B + R_D) + i_L R_D$$

$$-i_c/N_A = -I_{oA} + G_A e_1$$

$$i_{D2} = I_{oB} + G_B e_4$$

$$i_L(2R_D + R_L) + i_{D2}R_D - i_{D1}R_D = 0$$

4. Solution of the Modal Equations: The equations in the preceding section were solved simultaneously, each mode separately. When this was done, and the polarity of source voltage was inserted for each mode, the following results were obtained for core voltages and load current:

Mode I:

$$e_{1(I)} = \frac{E_{S1}/R_A - e_c/N_A R_c - I_{oA}}{1/N_A^2 R_c + G_A + 1/R_A}$$

$$e_{4(I)} = \frac{-N_B E_{S1}/N_B^2 R_A + I_{oB}}{1/N_B^2 R_A + G_B}$$

$$e_{2(I)},\ e_{3(I)},\ i_{L(I)} = 0$$

Mode II:

$$e_{3\,(II)} = \frac{-N_B E_{S1}/N_B^2 R_A + I_{oB}}{1/N_B^2 R_A + G_B}$$

$$e_{4(II)} = e_{3(II)}$$

$$e_{1(II)},\ e_{2(II)},\ i_{L(II)} = 0$$

Mode III:

$$e_{1(III)} = \frac{-e_c/N_A R_C + I_{oA}}{1/N_A^2 R_c + G_A}$$

$$e_{3(III)} = \frac{E_{S2}/(R_B + R_D) - I_{oB}}{1/(R_B + R_D) + G_B}$$

$$e_{4(III)} = e_{3(III)}$$

$$e_{2(III)},\ i_{L(III)} = 0$$

Mode IV:

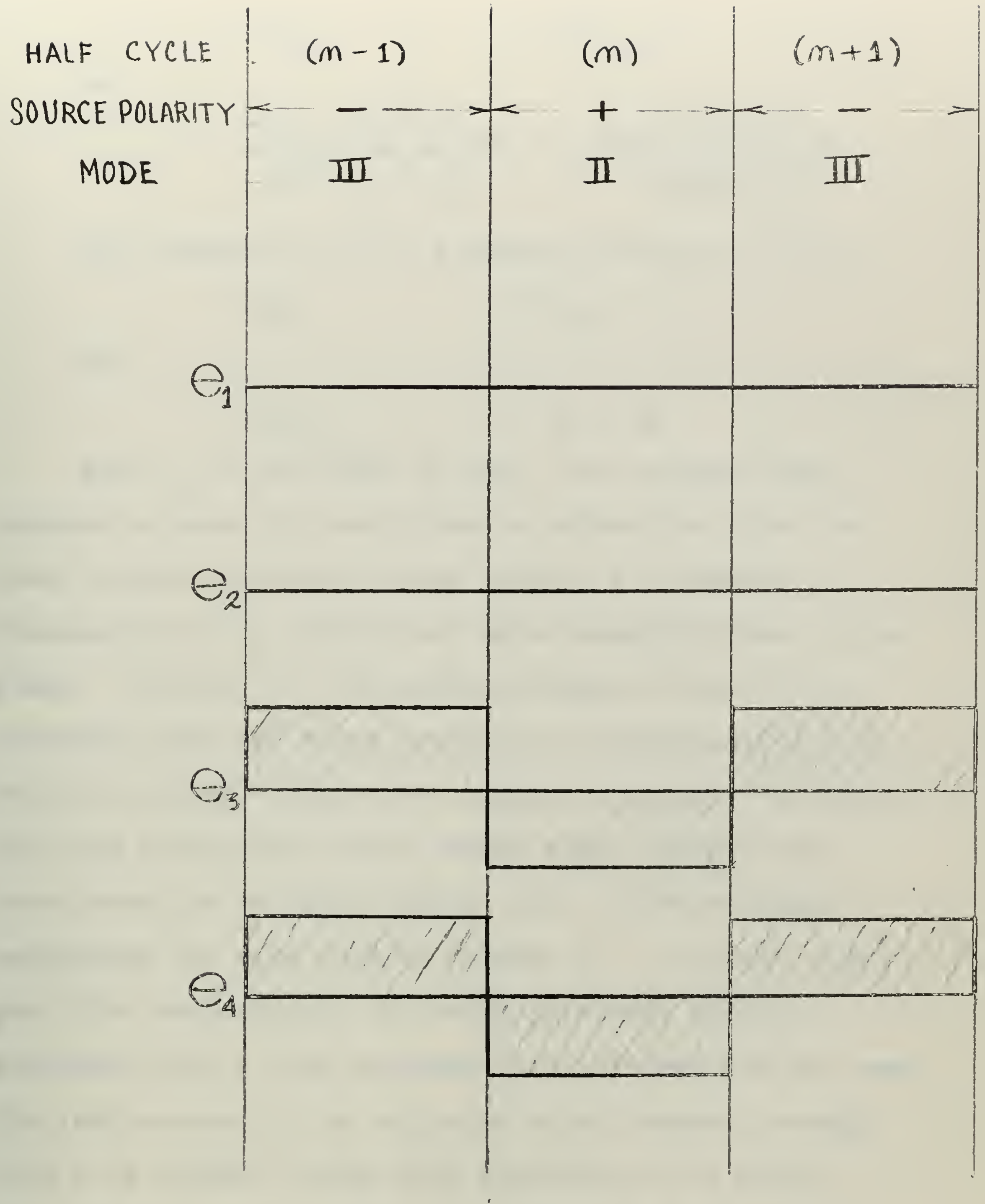
$$e_{1(IV)} = \frac{-e_c/N_A R_c + I_{oA}}{1/N_A^2 R_c + G_A}$$

$$e_{4}\ (IV) = \frac{\left[2R_D R_B + R_L R_B + R_L R_D\right]\left[E_{S2} - I_{oB}(R_B + R_D)\right]}{\left[2R_D R_B + R_L R_B + R_L R_D\right]\left[1 + G_B(R_B + R_D)\right] + R_D^2}$$

$$i_{L(IV)} = \frac{\left[R_D\right]\left[E_{S2} - I_{oB}(R_B + R_D)\right]}{\left[2R_D R_B + R_L R_B + R_L R_D\right]\left[1 + G_B(R_B + R_D)\right] + R_D^2}$$

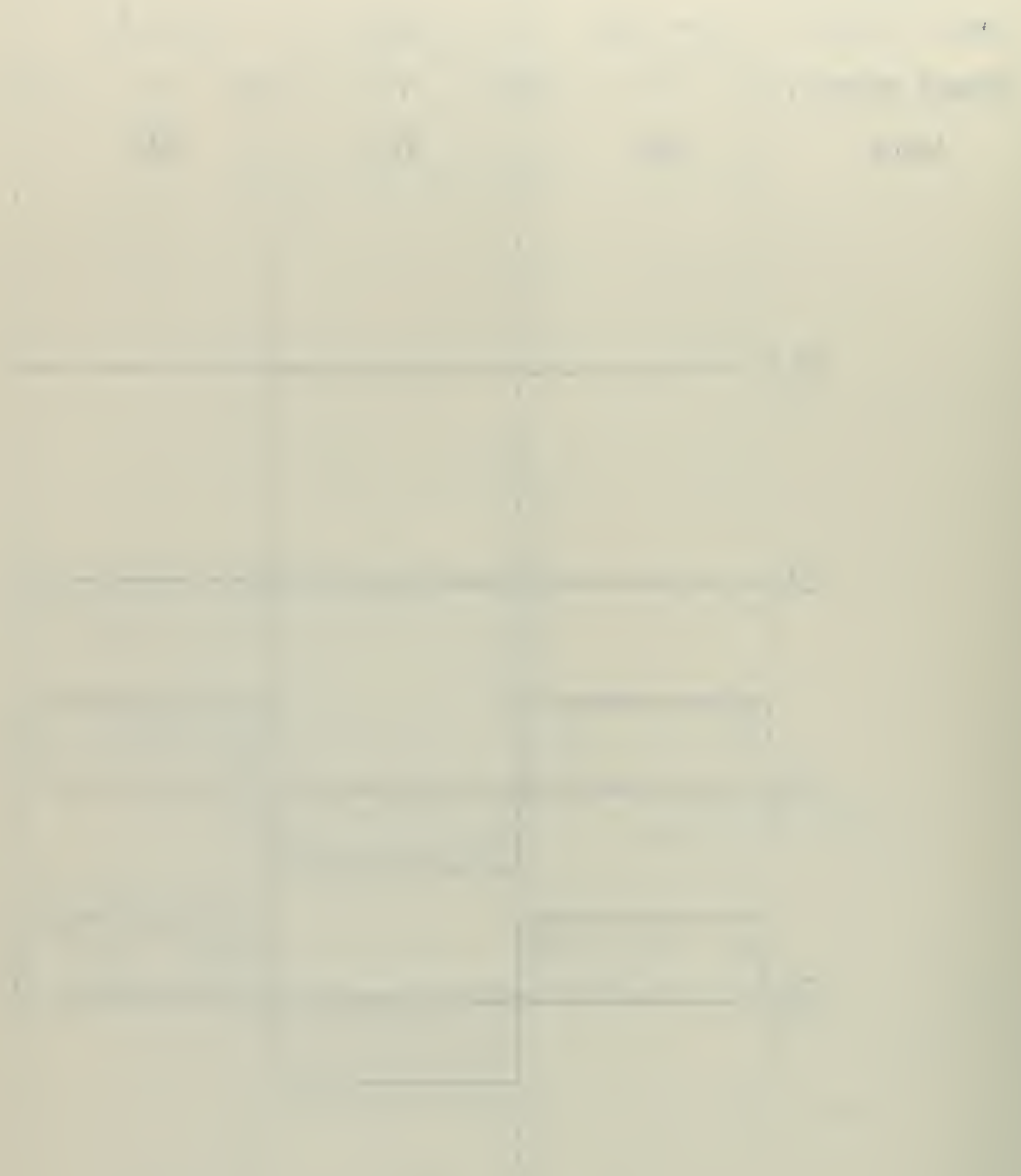
5. Reexamination of Circuit Operation, Based on Modal Solutions.

When $e_c = 0$, cores 1 and 2 must remain in saturation. In this condition, cores 3 and 4 alternate between the gate and reset values determined in Modes II and III, as shown in Fig. 3. In order that the output voltage be a minimum when there is no input voltage, it is necessary that the gate and reset values of voltage on these cores be equal in magnitude and opposite in polarity. If this is so, the output cores reach positive saturation at the end of one half cycle, negative saturation at the end of the next, and there is no load current. This is true if:



HYBRID III WAVEFORMS FOR $E_c = 0$

FIGURE 3



[illegible]

$$e_{3(II)} = -e_{3(III)}$$

or:

$$\frac{-N_B E_{s1}/N_B^2 R_A + I_{oB}}{1/N_B^2 R_A + G_B} = -\frac{E_{s2}/(R_B+R_D) - I_{oB}}{1/(R_B+R_D)+G_B}$$

One convenient way to accomplish this is to let:

$$N_B E_{s1} = E_{s2}$$

and:

$$N_B^2 R_A = R_B + R_D$$

When e_c is not equal to zero, the voltages were assumed to have the wave forms as solved for from the modal equations, and as shown in Fig. 4. However, examination of e_4 showed that this assumption must prove false. In Mode IV, the gating voltage of core 4 has decreased from the value previously determined for $e_c=0$ while the reset voltage has remained constant. In order that the volt second areas remain equal for gate and reset over the two half cycles, core 4 must saturate negatively for some portion of Mode II. It might seem that this would negate the modal solutions already performed, but it was reasoned that this was not the case. The load current is not effected since current through core 4 is blocked during this interval by its diode. The voltage on core 2 and the conditions in the input loop are not effected, since core 2 is already saturated. Therefore, the only change to the conditions originally assumed will be that the wave form of e_4 will be as shown in Fig. 5, and during the period when core 4 is

$$[illegible]$$

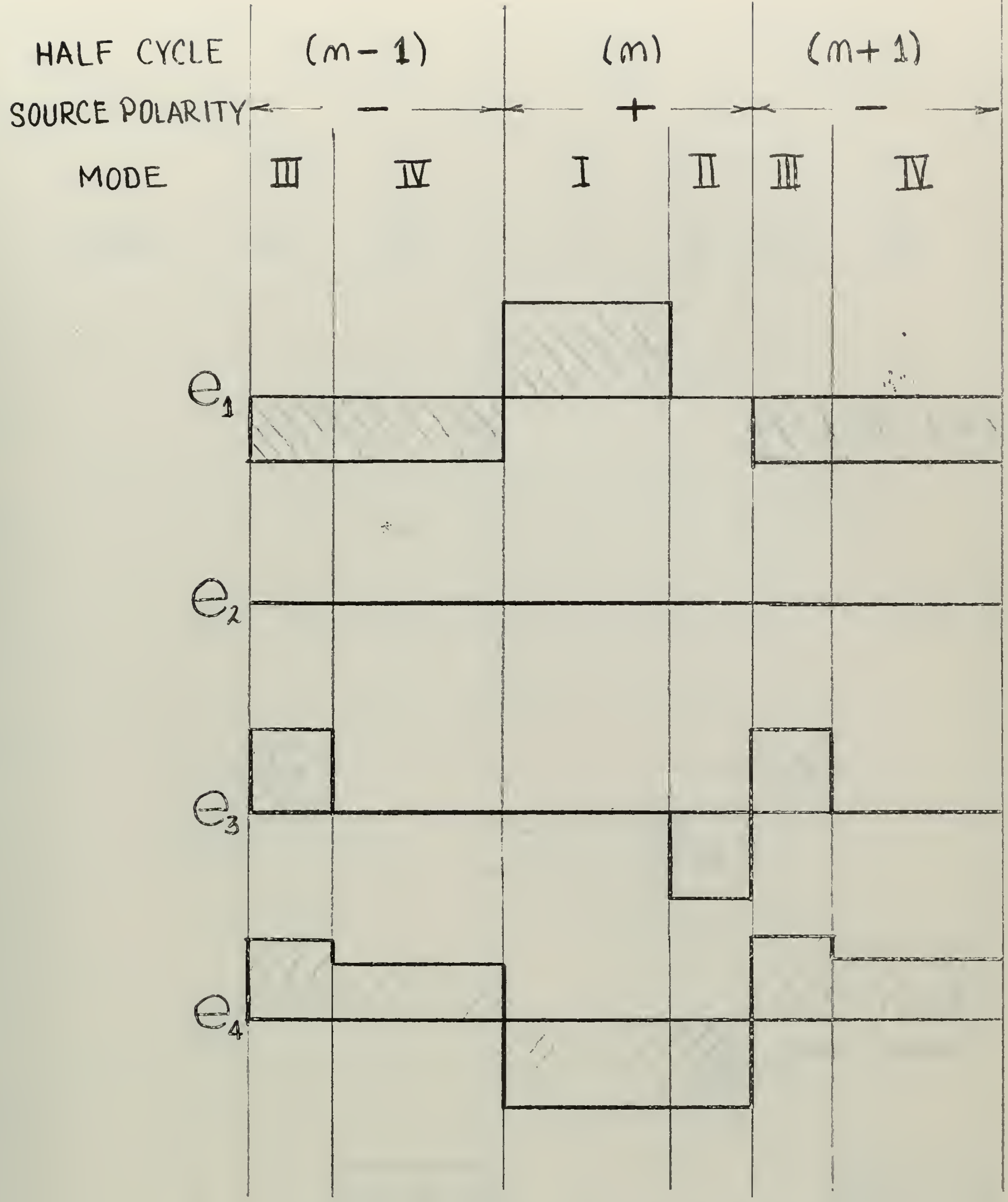
[illegible]

$$[illegible]$$

[illegible]

$$[illegible]$$

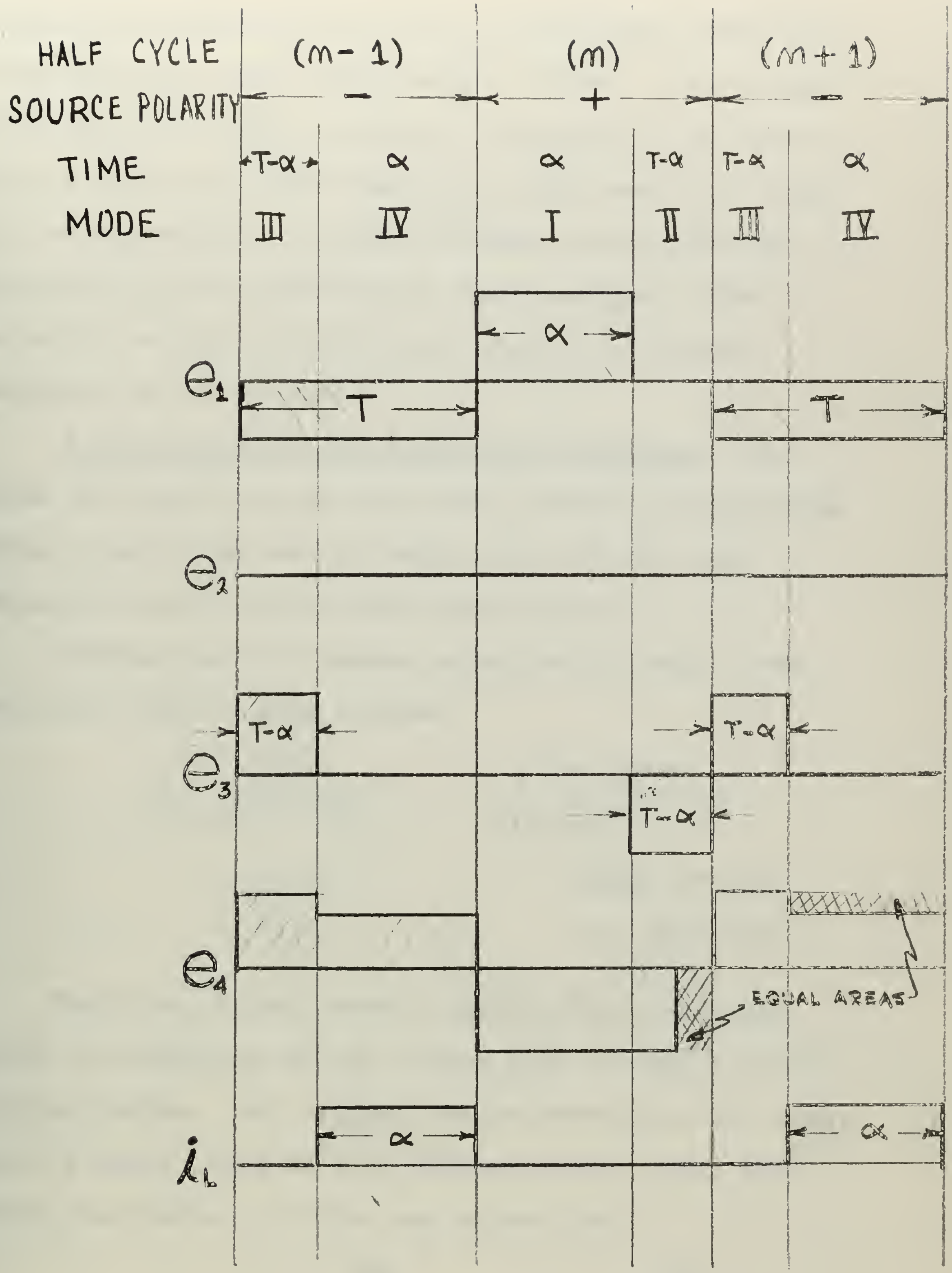
[illegible]



HYBRID III ASSUMED WAVEFORMS $E_c \neq 0$

FIGURE 4

[illegible]



HYBRID III REVISED WAVEFORMS $E_c \neq 0$

FIGURE 5

negatively saturated, all of E_{s1} will appear across R_A, resulting in a high instantaneous current. The gating time of core 3 (β) is shown to be equal to the reset time ($T - \alpha$) since the magnitudes have been made equal by the adjustment of supply voltages and resistances described in the beginning of this section. This is actually the first application of the volt second equation to the problem.

6. Derivation of the Difference Equation. Let Modes III and IV be the (n-1) half cycle, the following Modes I and II be the (n) half cycle and the next Modes III and IV be the (n+1) half cycle.

Writing the volt second equation for core 1 over the (n-1) and (n) half cycles:

$$\int_{(n-2)T}^{(n-1)T} e_{1(III)}\,dt + \int_{(n-1)T}^{(n-1)T+\alpha} e_{1(I)}\,dt = 0$$

$$e_{1(III)}T + e_{1(I)}\,(\alpha) = 0$$

$$e_{1(III)} + e_{(I)}\,\frac{\alpha}{T}(n) = 0$$

The time of load current flow in the (n+1) half cycle is controlled by the firing time of core 1 in the (n) half cycle. So, writing the expression of the half cycle average value of load current in the (n+1) half cycle, the value of $\alpha(n)$ was solved for:

$$I_{L(n+1)} = \frac{1}{T}\int_{T}^{2T} i_{L(n+1)}\,dt = \frac{1}{T}\int_{2T-\alpha}^{2T} i_{L(IV)}\,dt$$

[illegible]

[illegible]

[illegible]

$$[illegible]$$

[illegible]

[illegible]

[illegible]

$$[illegible]$$

$$= i_{L(IV)} \quad \frac{\alpha\,(n)}{T}$$

or:

$$\frac{\alpha\,(n)}{T} = \frac{I_{L(n+1)}}{i_{L(IV)}}$$

Next, the value of $\frac{\alpha\,(n)}{T}$ from the current equation was substituted into the volt second equation.

$$e_{1(III)} + e_{1(I)} \quad \frac{I_{L(n+1)}}{i_{L(IV)}} = 0$$

Finally, the known values from the modal solutions (with appropriate subscripts on E_c depending on the particular half cycle) were inserted in this equation. The equation was then simplified, and a difference equation resulted as follows, expressing output as a function of input:

$$I_{L(n+1)} = \frac{K_1 \frac{E_{c(n-1)}}{N_A R_c}}{K_2 - \frac{E_{c(n)}}{N_A Rc}} - \frac{K_1 K_3}{K_2 - \frac{E_{c(n)}}{N_A R_c}}$$

where:

$$K_1 = \frac{\left[\frac{1}{N_A{}^2 R_c} + G_A + \frac{1}{R_A}\right] \left[\frac{E_{s2}}{R_B+R_D} - I_{oB}\right] \left[R_D\right]}{\left[\frac{1}{N_A{}^2 R_c} + G_A\right] \left[\frac{R_D{}^2}{R_B+R_D} + \left(\frac{1}{R_B+R_D} + G_B\right) \left(2R_BR_D+R_LR_B+R_LR_D\right)\right]}$$

$$K_2 = \frac{E_{s1}}{R_A} - I_{oA}$$

$$K_3 = I_{oA}$$

Next, linearization of the difference equation was attempted. If $K_2 \gg E_{c(n)}/N_A R_c$ for the maximum value of E_c, then the difference equation can be reduced to the

form:

$$I_{L(n+1)} = \frac{K_1}{K_2} \frac{E_{c(n-1)}}{N_A R_c} - \frac{K_1 K_3}{K_2}$$

Maximum and minimum values were obtained as follows. The minimum value of $I_{L(n+1)}$ is 0, and will occur when $E_{c(n-1)}/N_A R_c$ is equal to I_{oA} (any less E_c will not have an effect on core 1). The maximum value of $I_{L(n+1)}$ will occur when $|e_{1(I)}| = |e_{1(III)}|$

or

$$\frac{\frac{E_c}{N_A R_c} + I_{oA} - \frac{E_{s1}}{R_A}}{\frac{1}{N_A{}^2 R_c} + G_A + \frac{1}{R_A}} = \frac{I_{oA} - \frac{E_c}{N_A R_c}}{\frac{1}{N_A{}^2 R_c} + G_A}$$

Solving for $E_c/N_A R_c$

$$\frac{E_c \text{ max.}}{N_A R_c} = \frac{\frac{E_{s1}}{R_A}\left(\frac{1}{N_A{}^2 R_c} + G_A\right) + \frac{I_{oA}}{R_A}}{\frac{2}{N_A{}^2 R_c} + 2G_A + \frac{1}{R_A}}$$

To check whether the transfer characteristic can be linearized, take a circuit:

$G_A = 10^{-4}$ $\quad N_B = 10$ $\quad E_{s2} = 100\text{v.}$

$G_B = 10^{-3}$ $\quad R_L = 1000\,\Omega$ $\quad E_{s1} = E_{s2}/N_B = 10\text{v.}$

$I_{oA} = 10^{-4}$ $\quad R_D = 750\,\Omega$ $\quad R_c = 10\,\Omega$

$I_{oB} = 10^{-3}$ $\quad R_B = 10\,\Omega$

$N_A = 10$ $\quad R_A = (R_B + R_D)/N_B{}^2 = 7.6\,\Omega$

then:

$$E_c \text{ max.}/N_A R_c = 10.9 \times 10^{-3}$$

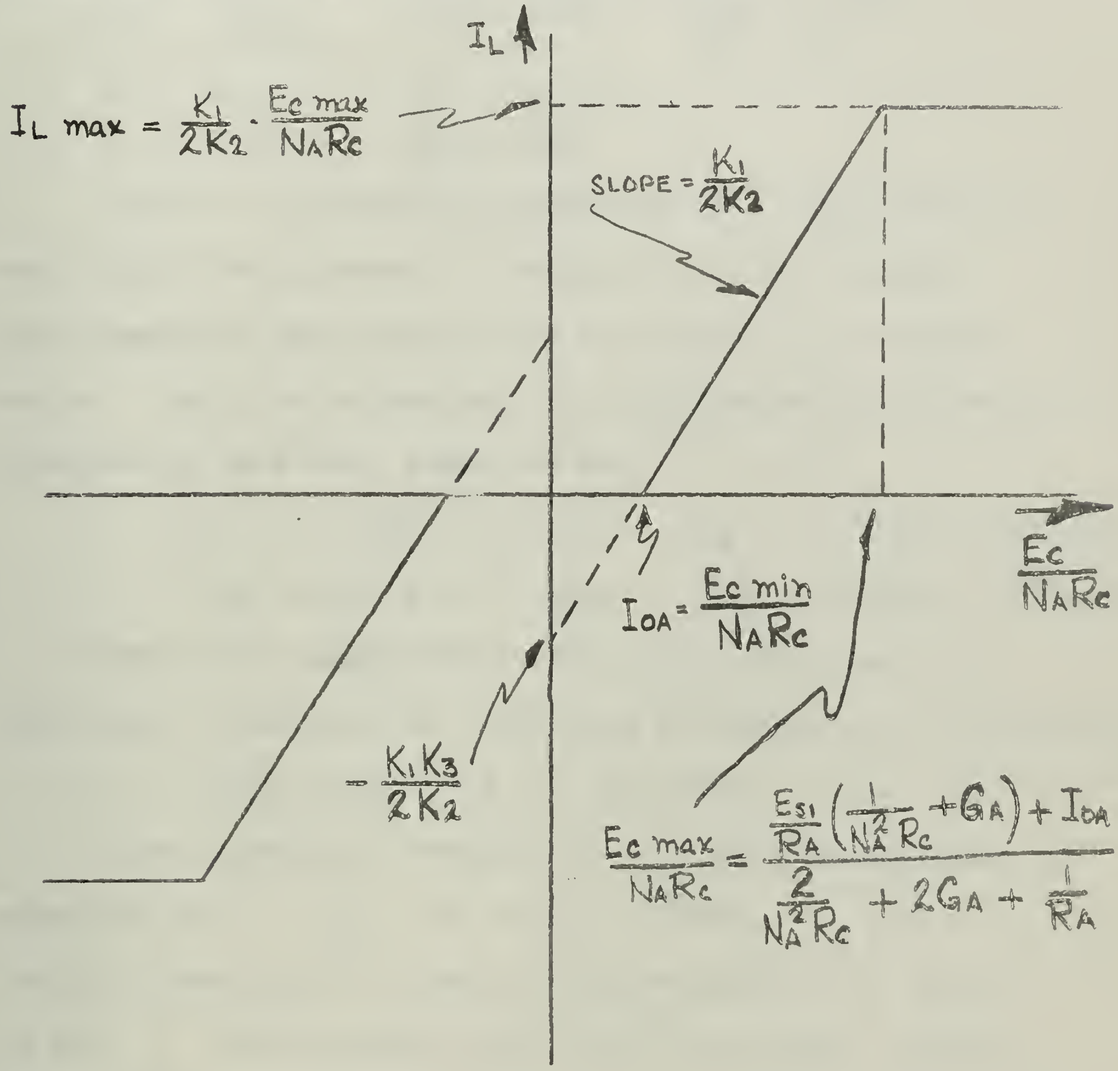
and:

$$K_2 = 999.9 \times 10^{-3}$$

thus $K_2 > E_c$ max.$/N_A R_c$ by two orders of magnitude, and it is valid to linearize the transfer characteristic to:

$$I_{L(n+1)} = \frac{K_1}{K_2} \quad \frac{E_{c(n-1)}}{N_A R_c} - \frac{K_1 K_3}{K_2}$$

This results in a linearized steady state transfer characteristic as shown in Fig. 6. The I_L plotted is the full cycle average value of i_L and this is just one half the half cycle average value of load current which appears in the difference equation.



HYBRID III LINEARIZED TRANSFER CHARACTERISTIC

FIGURE 6

[illegible]

[illegible]

7. Experimental Verification of Analysis. The next step was to build the circuit and to attempt to verify the difference equation and transfer characteristic that had been obtained. The circuit was set up as shown in Fig. 1. Parameter values were as follows:

$R_L = 1280\,\Omega$ $\quad n_{cA} = 90T$ $\quad n_{gA} = 450T$
$R_D = 890\,\Omega$ $\quad n_{cB} = 125T$ $\quad n_{gB} = 1000T$
$R_A = 15.035\,\Omega$ $\quad N_A = 5$ $\quad N_B = 8$
$R_B = 20\,\Omega$ $\quad E_{s1} = 5.8v.$
$R_c = 100\,\Omega$ $\quad E_{s2} = 24v.$

Source resistance was measured at 1.435 ohms and was taken into account by adding it to the winding resistance of the center loop to obtain R_A as shown above. The core parameters were determined as shown in Appendix A, and were found to be:

$G_A = .0868 \times 10^{-3}\,\mho$ $\qquad G_B = .0763 \times 10^{-3}\,\mho$
$I_{oA} = .35 \times 10^{-3}$ amps $\qquad I_{oB} = 1.065 \times 10^{-3}$ amps

Using the parameters in the previously derived difference equation the following constants were determined:

$K_1 = 1.359$ amps $\qquad K_2 = .339$ amps $\qquad K_3 = .35 \times 10^{-3}$ amps

These constants resulted in a steady state gain equation of: $E_L = 5.12\,E_c - .904v.$ and a complete analytical transfer characteristic as shown in Fig. 7. Experimental data was then taken, and was also plotted on Fig. 7.

There are several things worth noting from the comparison of the analytical and experimental transfer characteristics:

[illegible]

$$[illegible]$$

[illegible]

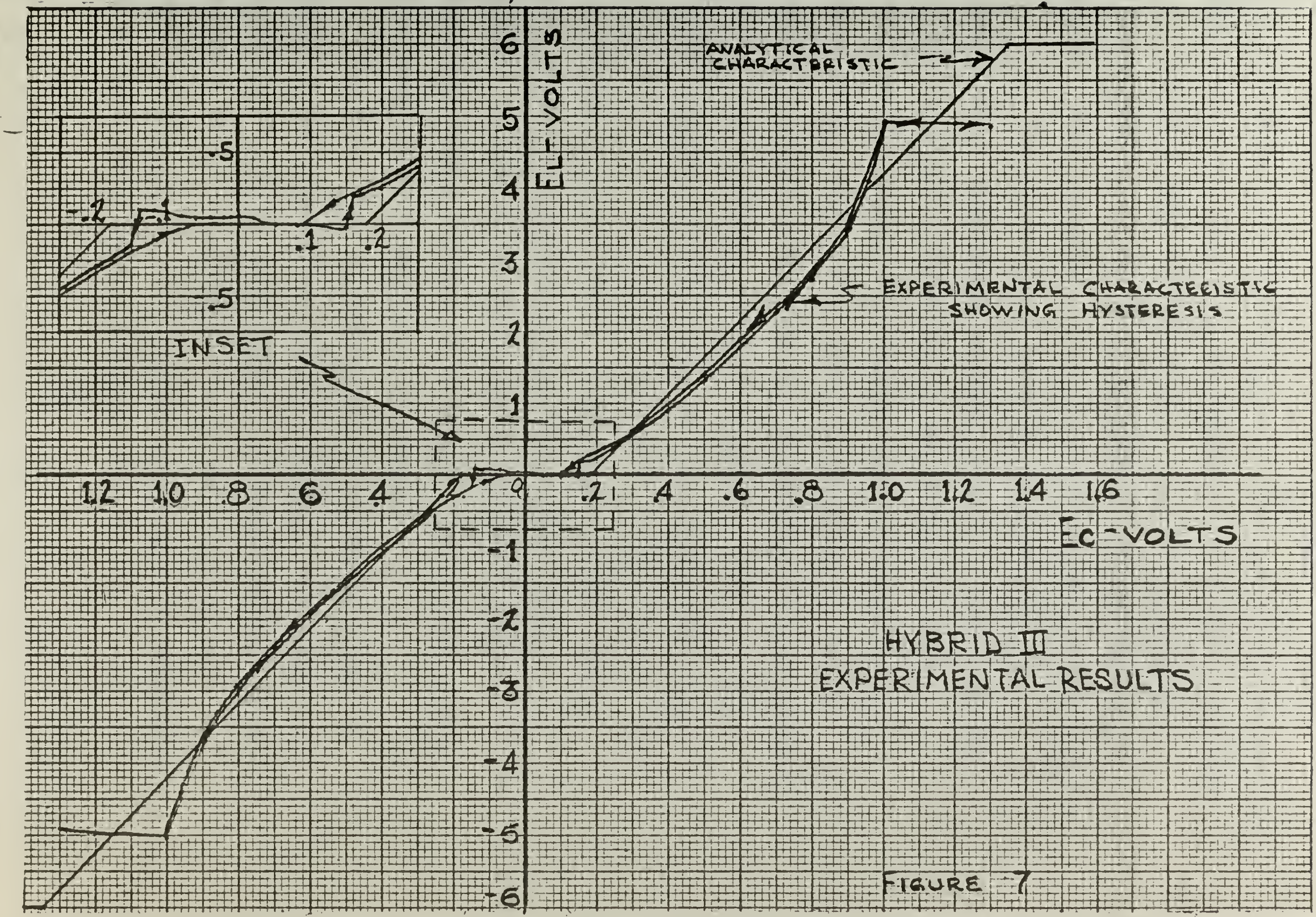
$$[illegible]$$

[illegible]

[illegible]

[illegible]

[illegible]



HYBRID II
EXPERIMENTAL RESULTS

FIGURE 7

(1) In general, the experimental gain agreed well with that which was analytically determined, except for a gradual increase in gain as the output was increased. The reason for this will be discussed in a later section.

(2) The jump discontinuity, close to the origin in believed to be due to "triggering" of the output cores. This phenomenon is discussed in references 3 and 4.

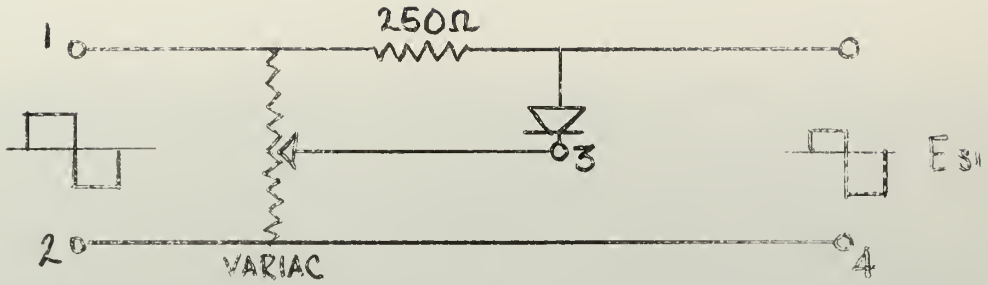
(3) The discrepancy between experimental and analytically determined maximum output is believed to be due to diode unblocking in the output circuit. Consider the output core which does not saturate because of E_c (core 4 for polarity as shown in Fig.1). If, during the half cycle when i_D is supposed to be blocked be the output diode, the core couples across to the output circuit enough of E_{s1} to more than equal E_{s2}, current will flow in this loop when it was assumed not to, in the original modal assumptions. This current will produce a voltage across the output which is opposed to the normal polarity of output voltage. When the output voltage is averaged over a full cycle, this results in a reduced d.c. output.

The next step of experimental verfication was to employ a non-symmetrical supply voltage to attempt to eliminate diode unblocking. Although unblocking was believed to be occurring in both the coupling and output circuits, it was decided to attempt to eliminate it at first only in the coupling circuit.

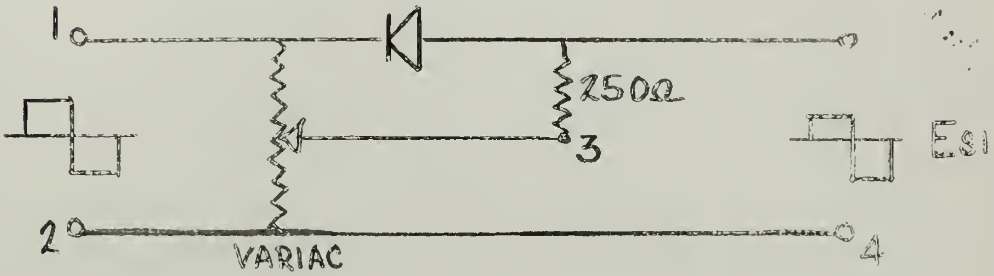
A non-symmetrical voltage can be developed using either circuit A or circuit B of Fig. 8. However, it was postulated that circuit A would have low source impedance during the positive half cycle and high impedance during the negative half cycle, while B would have high source impedance in the positive half cycle and low source impedance in the negative half cycle. Since low source impedance is a generally desirable characteristic for the supply voltage to any magnetic amplifier, and since the external amplifier circuit is designed to prevent current flow during the negative half cycle, circuit A was chosen.

To verify this hypothesis, the circuit shown in Fig. 9 was devised to measure the source impedance in the forward direction for both circuits A and B. By measuring the forward voltage on the oscilloscope it was found that for circuit A, the forward impedance was 21.8 ohms., while that of circuit B was 213 ohms. Thus the advantage of circuit A was verified.

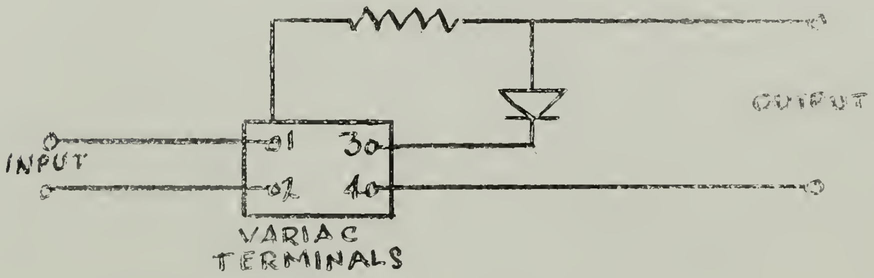
Next, using circuit A for the generation of E_{s1}, new experimental data was taken which, it was expected, would more nearly equal the theoretically derived transfer characteristic. Unfortunately, this was not the case. The results are shown in Fig. 10. All parameters were the same, except for the addition of the non-symmetrical E_{s1}, which resulted in a slight



CIRCUIT A



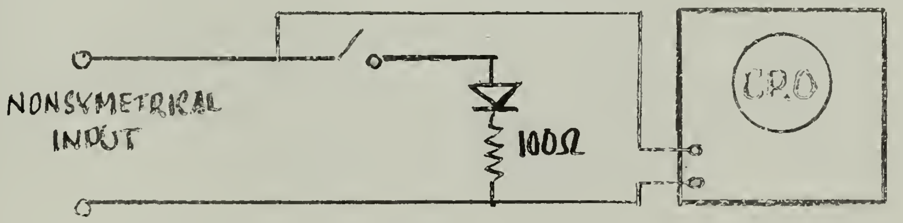
CIRCUIT B



WIRING DIAGRAM OF CIRCUIT A

CIRCUITS FOR GENERATION OF NONSYMETRICAL VOLTAGES

FIGURE 8

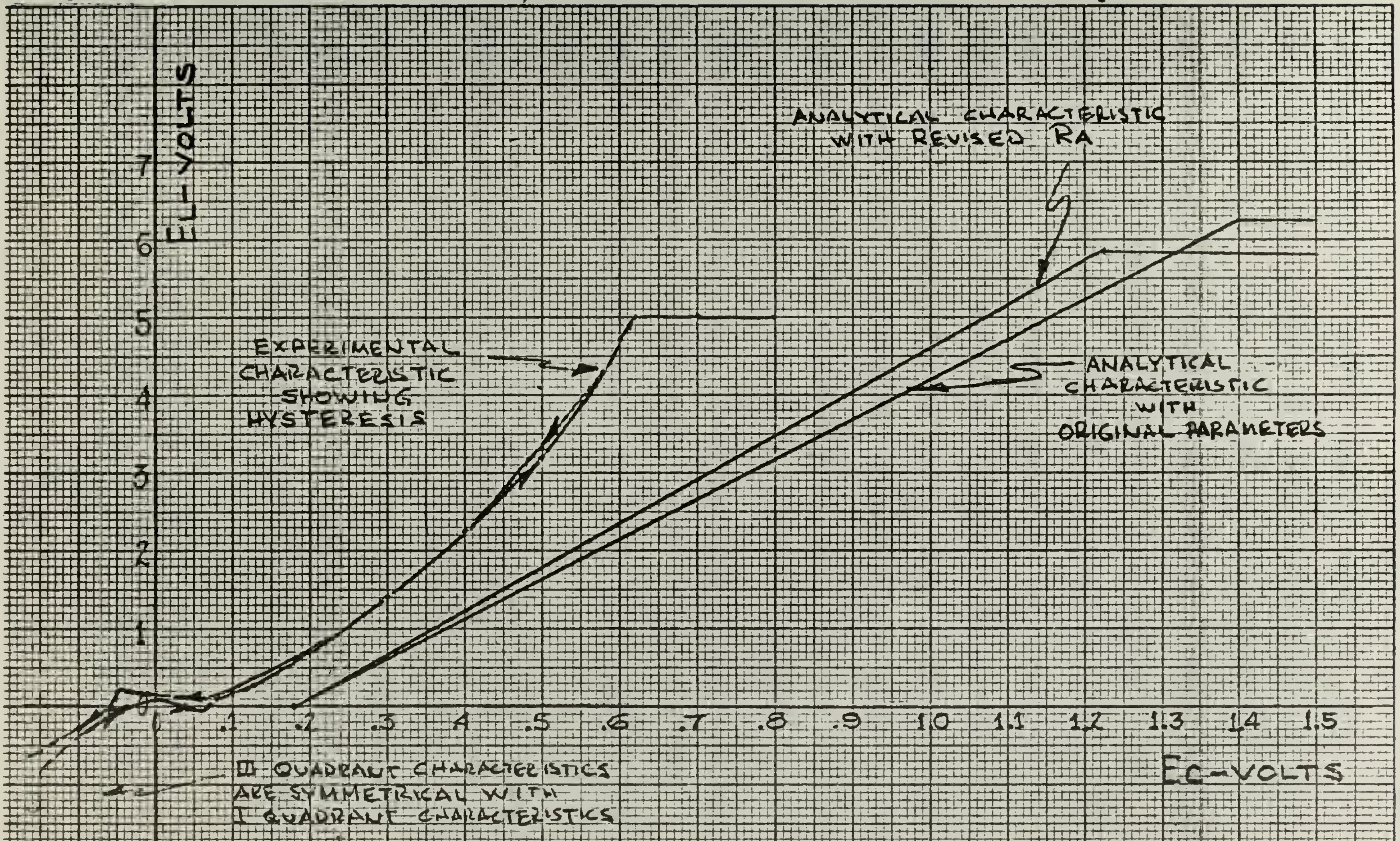


CIRCUIT FOR MEASURING FORWARD SOURCE IMPEDANCE

FIGURE 9

[illegible]

[illegible]



EXPERIMENTAL RESULTS USING NONSYMMETRICAL SOURCE VOLTAGE

FIGURE 10

adjustment of the forward magnitudes of E_{s1} and E_{s2} (E_{s1} = 4.6v., E_{s2} = 23.5v.). The analytical transfer characteristic was derived in two ways, as shown on the figure, for comparison. First, all the original parameters were used, ignoring the 21.8 ohms source resistance and the voltage variations. This resulted in a serious discrepancy between experimental and analytical results. Next, the new values were taken into account. R_A was the parameter most seriously effected. It was modified by making the assumption that equal currents flowed in the two coupling loops (an assumption that was far from true, as will be shown later). With this assumption it was possible to modify R_A by simply adding twice the source impedance to it. This was done, and the resulting analytical transfer characteristic was, although closer than with the original parameters, still far from the experimental results.

8. Reexamination of Circuit Operation, Considering Negative Saturation of an Output Core.

After the unsatisfactory experimental results that were obtained when source resistance was introduced into the coupling loop, it was deemed advisable to completely reexamine the assumed modes of operation of the circuit.

It is recalled here that one of the original assumptions made was that the source impedance of

[illegible]

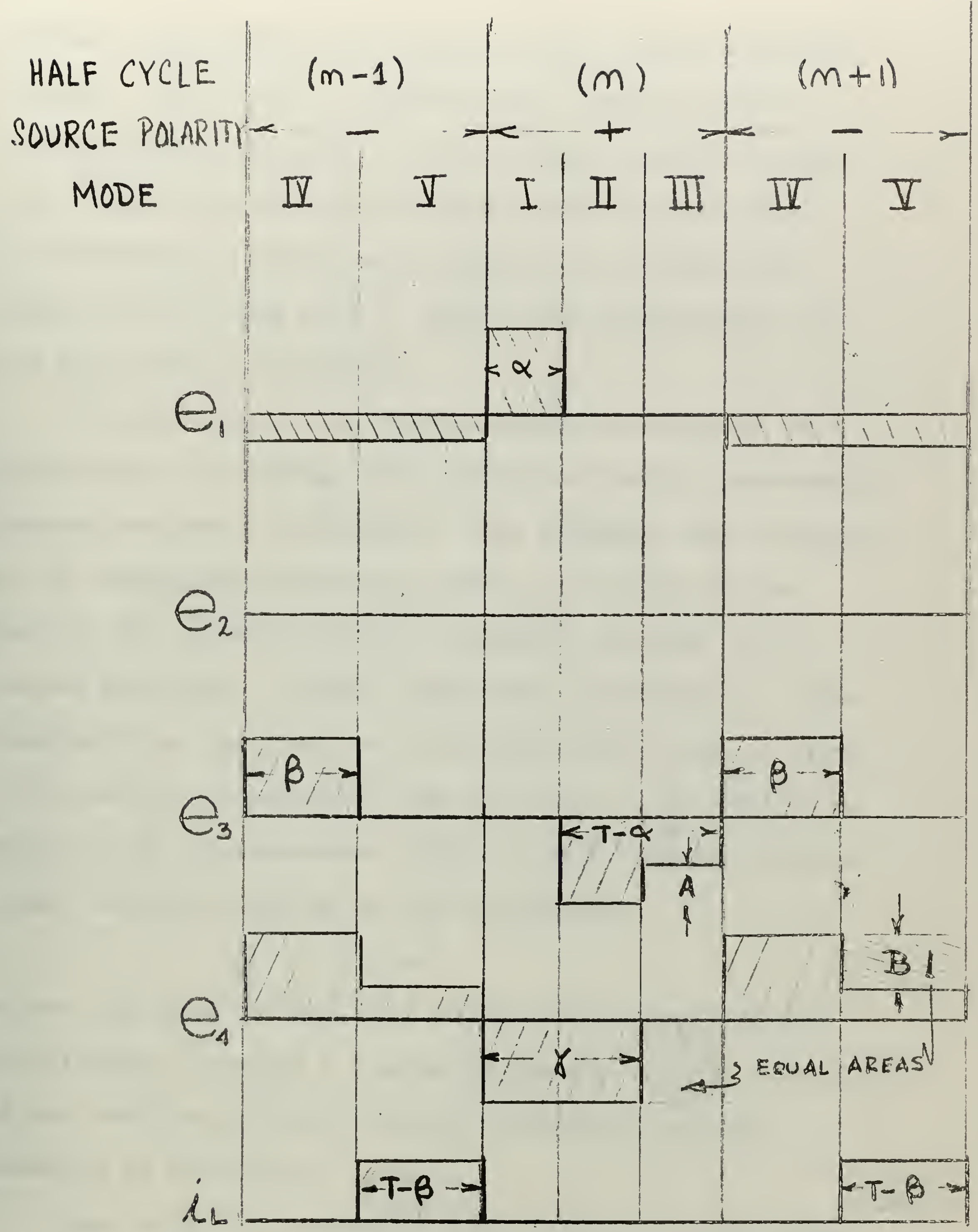
[illegible]

[illegible]

[illegible]

both E_{s1} and E_{s2} were negligible. At this point, this assumption was dropped, and a new qualitative examination of circuit operation was made, starting from the point in section 5 where it was discovered that, for a non-zero input voltage with polarity shown in Fig. 1, core 4 saturates negatively during some portion of its reset half cycle.

The operation under these conditions is best understood by referring to Fig. 11. The modes of operation have been re-numbered to include that in which core 4 saturates negatively. In this mode (III) a large current will flow through cores 2 and 4, limited only by R_A and the source resistance of E_{s1}. If this source resistance is appreciable compared to R_A (it was greater than R_A in the experimental setup) the voltage applied to the upper loop (cores 1 and 3) will be appreciably reduced in this mode. Since core 1 is saturated at this time, this reduced voltage is that which is applied to core 3 for reset. This will result in a smaller volt-time area and a consequently smaller flux reset during the reset half cycle. In the next output half cycle, core 3 will therefore saturate earlier, and the half cycle average of output current will be increased. This in turn will lead to an earlier reduction of core 4 gating voltage in Mode V, a consequent earlier negative saturation of core 4 in the next half cycle, and a continuation of the



A - REDUCTION OF VOLTAGE DUE TO SOURCE VOLTAGE AND HIGH CURRENT IN OPPOSITE LOOP

B - REDUCTION OF VOLTAGE DUE TO OUTPUT CIRCUIT CONFIGURATION

HYBRID III WAVEFORMS
INCLUDING EFFECTS OF SOURCE RESISTANCE

FIGURE 11

process, increasing the output, until steady state is reached. This then , explains the remarks in the introduction concerning the non-linear positive feedback effect and the loss of one cycle response time. The feedback is non-linear because the amount will depent on how long Mode V lasts, and consequently on how long Mode III exists.

It can now be seen that a complete analysis of the circuit, including the effects of source resistance, becomes extremely difficult. The voltages and currents in the individual modes can still be solved for as before, but relating input to output, through volt-second equations, becomes much more complicated. This results from the fact that the saturation time of core 1 (α) and the saturation time of core 3 (β)(which is equal to the commencement time of load current) are no longer simply relating by the expression

$$\beta = T - \alpha$$

as was the case in Fig. 5. In the new situation the relationship between $T - \alpha$ and β depends on the magnitude of the coupling circuit source resistance and the duration of Mode III.

The following procedure would have to be followed for a complete analysis of the circuit, including the effects of source resistance: (refer to Fig. 11)

(1) Solve for e_1, e_3, and e_4, in each of the five modes.

(2) From a volt second equation for core 4, find the relationship between negative saturation time (γ) and load current firing time (β) in terms of half cycle average output current.

(3) From a volt second equation for core 3, find the relationship between $T - \alpha$ and β.

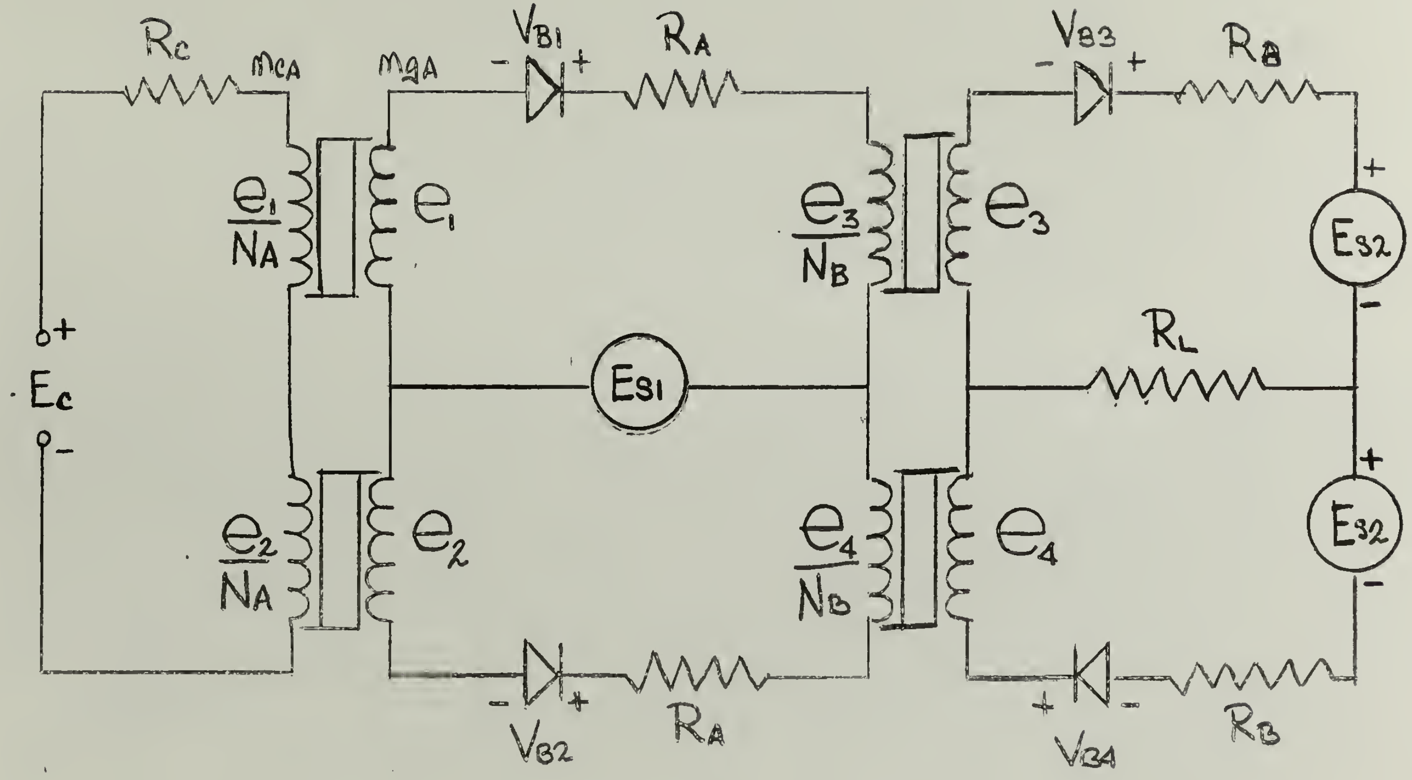
(4) From a volt second equation for core 1, find the relationship between α and input voltage.

(5) By inter-relating the above steps, find the difference equation which relates input to output.

This procedure was started, and those solutions that were obtained are contained in Appendix B, for anyone who may wish to pursue the analysis.

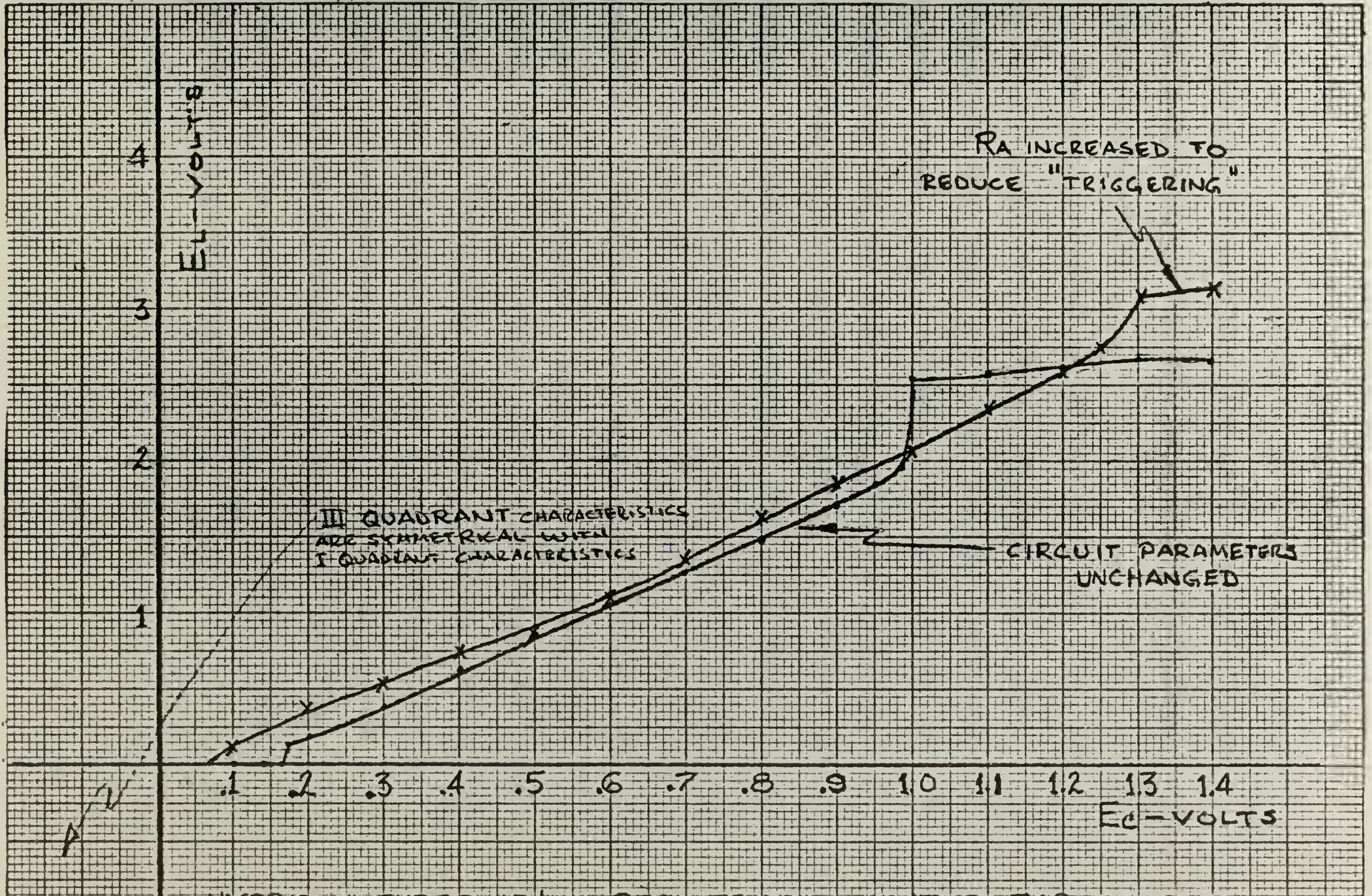
9. Experimental Verification of Section 8, and Conclusion.

The positive feedback effect which has just been discussed was believed to be the cause of the slight upward curve of the transfer characteristic before extra source resistance was added by the non-symmetrical source circuit. (Fig. 7). The source resistance in this case was only 1.435 ohms, but this becomes significant when compared to $R_A = 13.6$ ohms. To verify that this effect was the cause of the gain increase, it was decided to modify the output circuit so that no negative saturation of an output core would take place. This was accomplished by using a center-tap output, as shown in Fig. 12. The general characteristics of the circuit are the same as before. It has a half wave, push-pull output.



HYBRID III WITH CENTER-TAP OUTPUT
FIGURE 12

[illegible]



HYBRID III EXPERIMENTAL RESULTS USING CENTER-TAP OUTPUT
FIGURE 13

The experimental setup used the same parameters as those which resulted in Fig. 7. The positive feedback effect resulting in the upward curve of the characteristic was expected to be eliminated. Because of the change in configuration of the output circuit, it was not expected that the gain would equal that obtained previously.

The results obtained are shown in Fig. 13. It can be seen that the positive feedback effect was eliminated, but there was a jump discontinuity near maximum output. It is believed that this is due to "triggering" of the input cores. This phenomenon is well discussed in reference 3 and 4. The effect was largely eliminated by increasing the resistance in the coupling loop, as shown in the second curve of Fig. 13.

It can be concluded from this analysis and the preceding discussion, that the complete analysis of the Hybrid III magnetic amplifier is an extremely lengthy task. It is not a technically difficult task, however, only requiring much time consuming continuation of the work that has been done here. However, if an analysis which assumes negligible source impedance will serve the purposes of the designer, it is believed that the results contained in section 6 will closely match future experimental data.

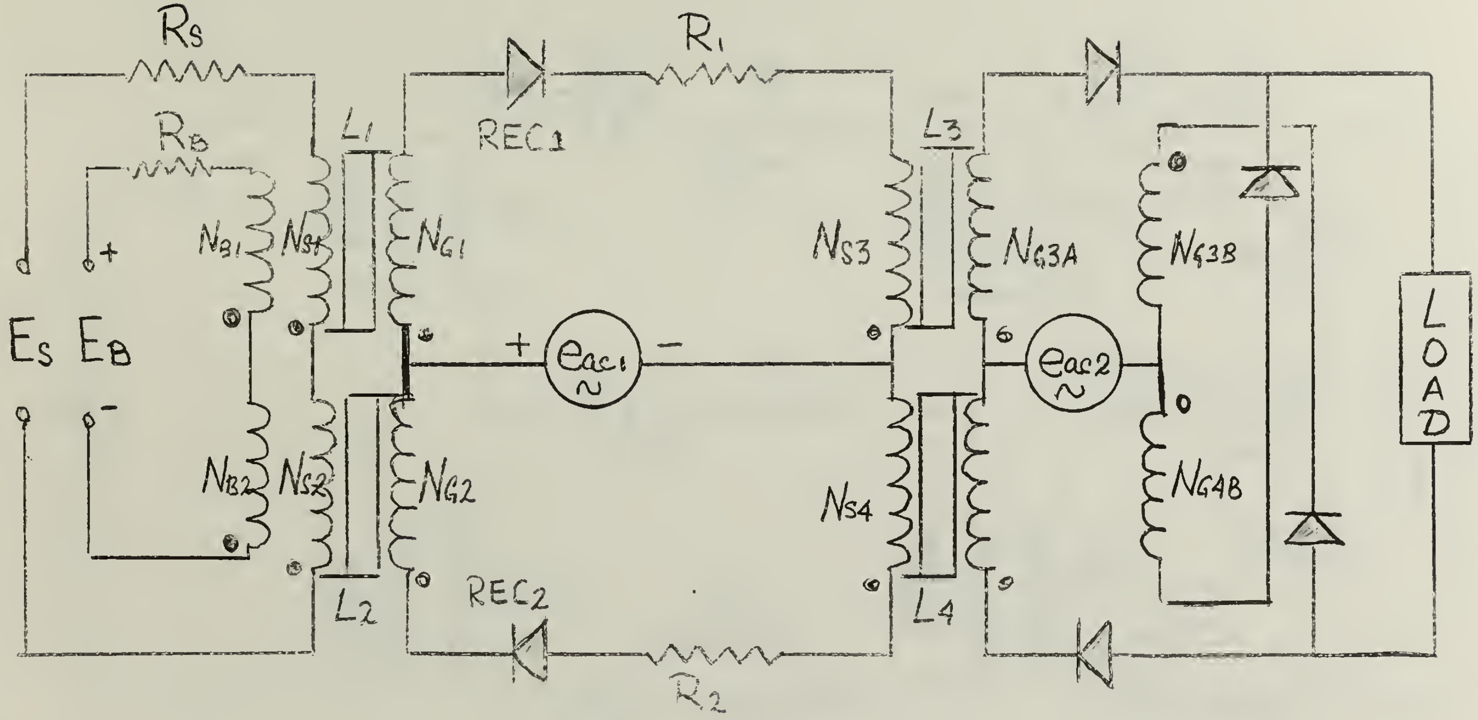
III

THE HYBRID IV AMPLIFIER

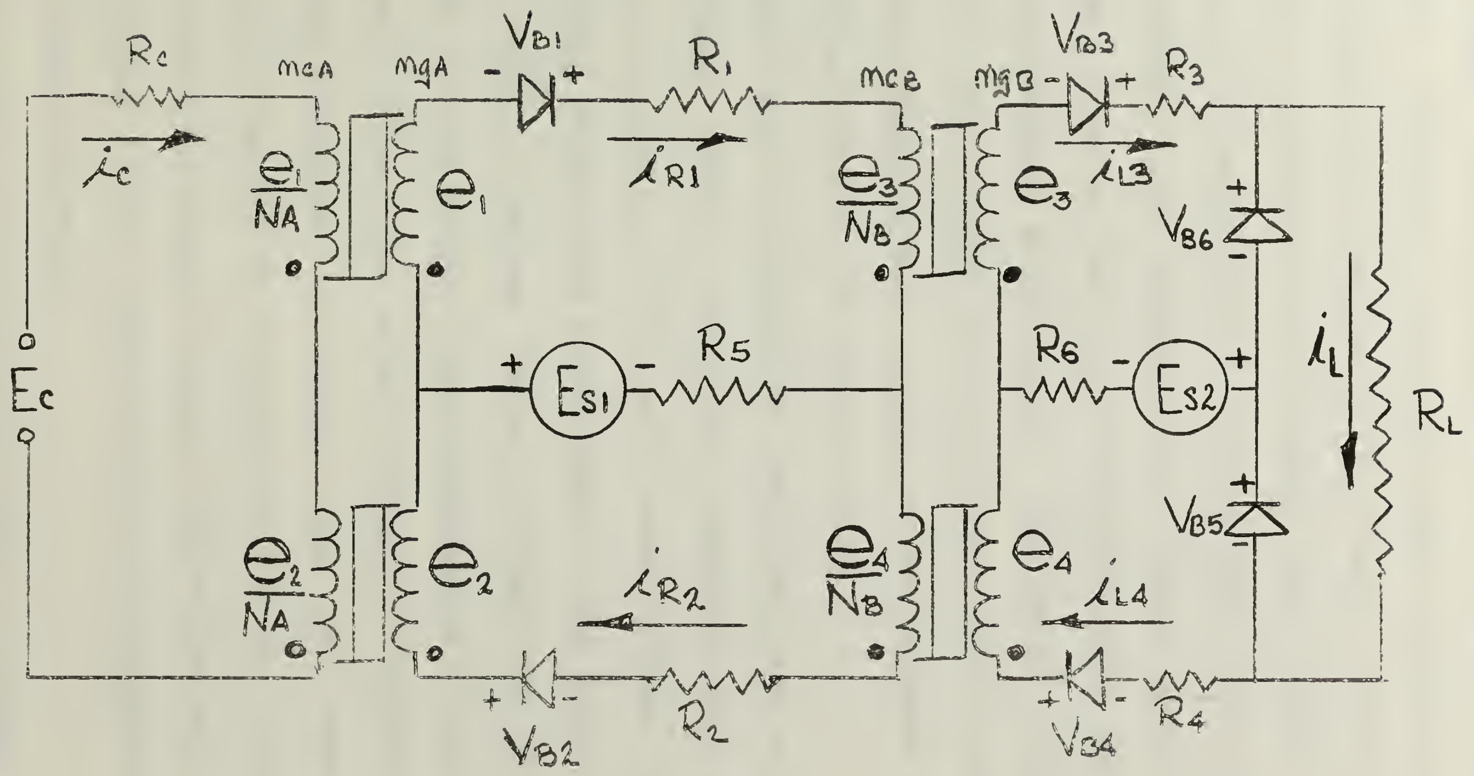
A. Introduction and Description.

The Hybrid IV magnetic amplifier circuit as usually configured is shown in Fig. 14. A simplified form, which is equivalent for analysis purposes, is shown in Fig. 15. The number of turns in the gating winding of an output core of Fig. 15 is equal to the sum of the turns on both gating windings of the output core in Fig. 14. As in the Hybrid III, this circuit will accept a phase reversible a.c. input but it will only accept one polarity of d.c. input, and it will provide a phase reversible a.c. output or an unidirectional d.c. output. The output contains a variable d.c. component which is often desirable for damping in dynamic control applications. Examination of the circuit reveals that the input and output cores gate in alternate half cycles. This results in a full wave output at maximum input, which means greater inherent gain than that of the Hybrid III, but also means a loss of the latter's fast response time, because of coupling between the upper and lower portions of the circuit through the input loop.

A description of the circuit's operation is as follows. It can be seen that because of the arrangement of the diodes in the coupling loop, cores 1 and 2 can



CIRCUIT DIAGRAM FOR A HYBRID IV AMPLIFIER
FIGURE 14



HYBRID IV CIRCUIT - SIMPLIFIED FOR ANALYSIS

FIGURE 15

[illegible]

receive gating voltage only from the coupling loop source voltage, and they receive this voltage in alternate half cycles. Likewise, the output cores receive their gating voltages only from the output source voltage, and they also receive it in alternate half cycles. It is assumed, and the circuit is so designed, that the current flowing in the coupling loop before saturation of the input core in that loop is insufficient for reset of the corresponding output core. The amount of reset of an output core depends on the firing time of the input cores, which in turn depends on the amounts of reset provided them by the input voltage.

Consider now the situation resulting from zero input voltage. Cores 1 and 2 will saturate early in alternate half cycles, their only reset voltage coming from coupling through the input loop to one input core while the other is gating. Reset voltage will therefore be provided to the output cores alternately, over most of each half cycle. The output voltage is adjusted so that in this condition the output cores just reach saturation at the end of a gating half cycle. This results in minimum output current, since the only current flowing in the output loop is the magnetization current before saturation.

If the input voltage is now slowly increased, the time of saturation of cores 1 and 2 will be later and later, since they are receiving more reset voltage.

This means that cores 1 and 2 will take longer to gate to saturation, thus allowing less time for reset current to flow in cores 3 and 4. This in turn will mean that the firing times of cores 3 and 4 will become earlier, allowing output current to flow during a greater portion of each half cycle, thereby increasing its average value. There will be a minimum input voltage above which the output core undergoing gating will saturate before the input core which is gating during the same half cycle. This will result in two possible sequences of operation. Either the input core will saturate prior to the output core diagonally opposite it, or this output core will saturate first. It will be shown in the analysis that both situations lead to the same results. In other words, the Hybrid IV is a balanced circuit since, during steady state operation, cores 1 and 4 in one half cycle perform identically to cores 2 and 3 respectively in the alternate half cycle.

B. The Analysis

1. Assumptions. The general method of analysis is the same as in section B of part I. The circuit used in this analysis has been shown in Fig. 15. Definitions of parameters are the same as those for the Hybrid III (Fig. 2) with the following exceptions:

R_1, R_2 = Resistances of coupling loop, less source but including core windings and forward diode resistance.

R_3, R_4 = Resistance of output loop, less source and load resistances but including winding and two forward diode resistances.

R_5, R_6 = Source resistance.

$R_A = R_1 + R_5 = R_2 + R_5$

$R_B = R_3 + R_6 + R_L = R_4 + R_6 + R_L$

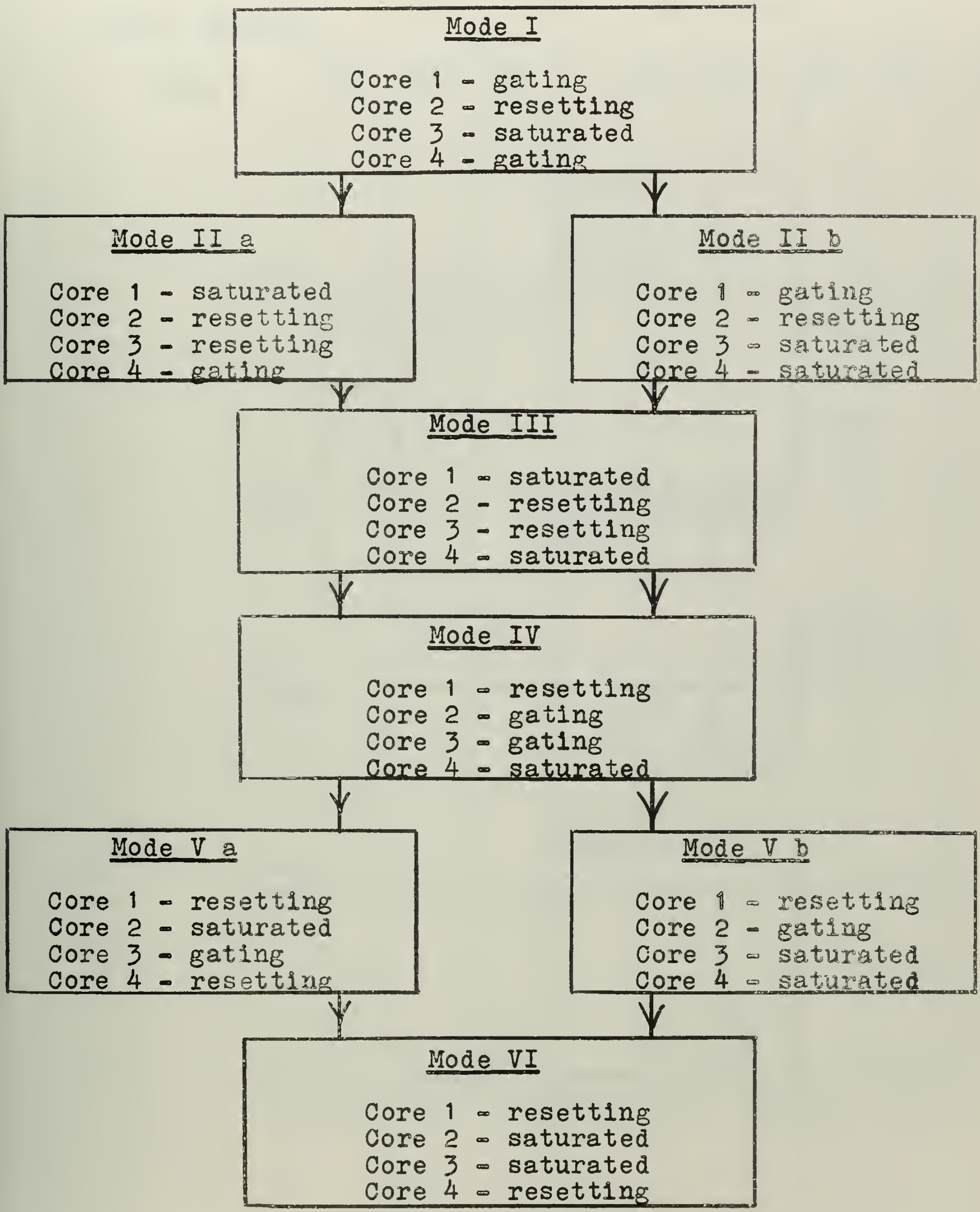
The same assumptions apply as were made for the Hybrid III, with the following exceptions:

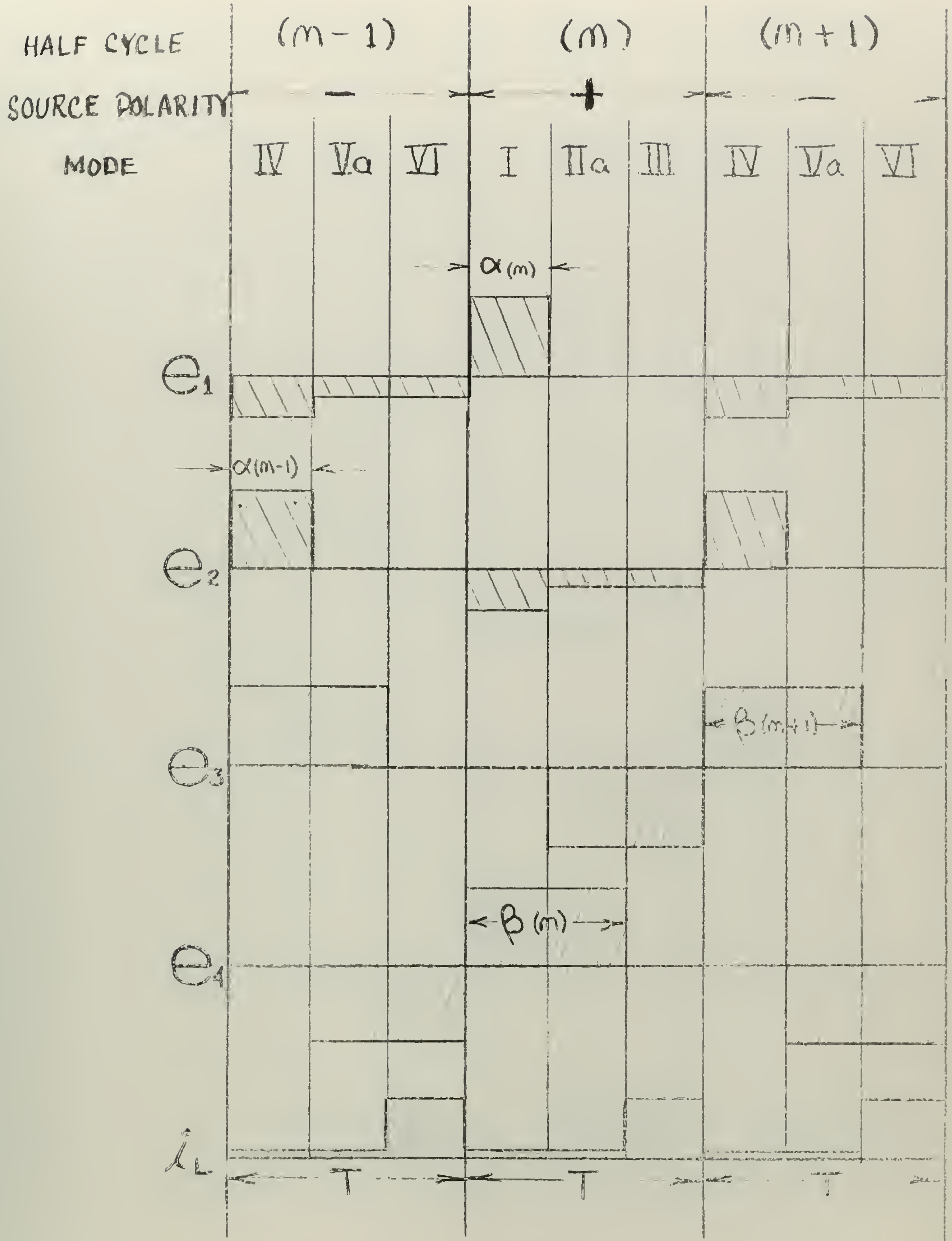
The source voltages are not assumed to have negligible source resistances.

When a pair of output diodes such as 3 and 5 are not conducting, the voltage across the pair divides equally between them.

2. Assumed Modes of Operation. Based on the description of circuit operation in section A, it was assumed that modes of operation are as shown in the table of Fig. 16. There are two possible paths through the modes, either down through the left half or through the right half of the figure. These two possibilities are shown in the waveforms of Fig. 17 and 18. It can be seen that for either of the two paths, modes IV, V, and VI are the same as I, II, and III respectively, if core 1 is interchanged with core 2 and core 3 with core 4. This will simplify the analysis, in that explicit modal solutions need only be obtained for the first three modes.

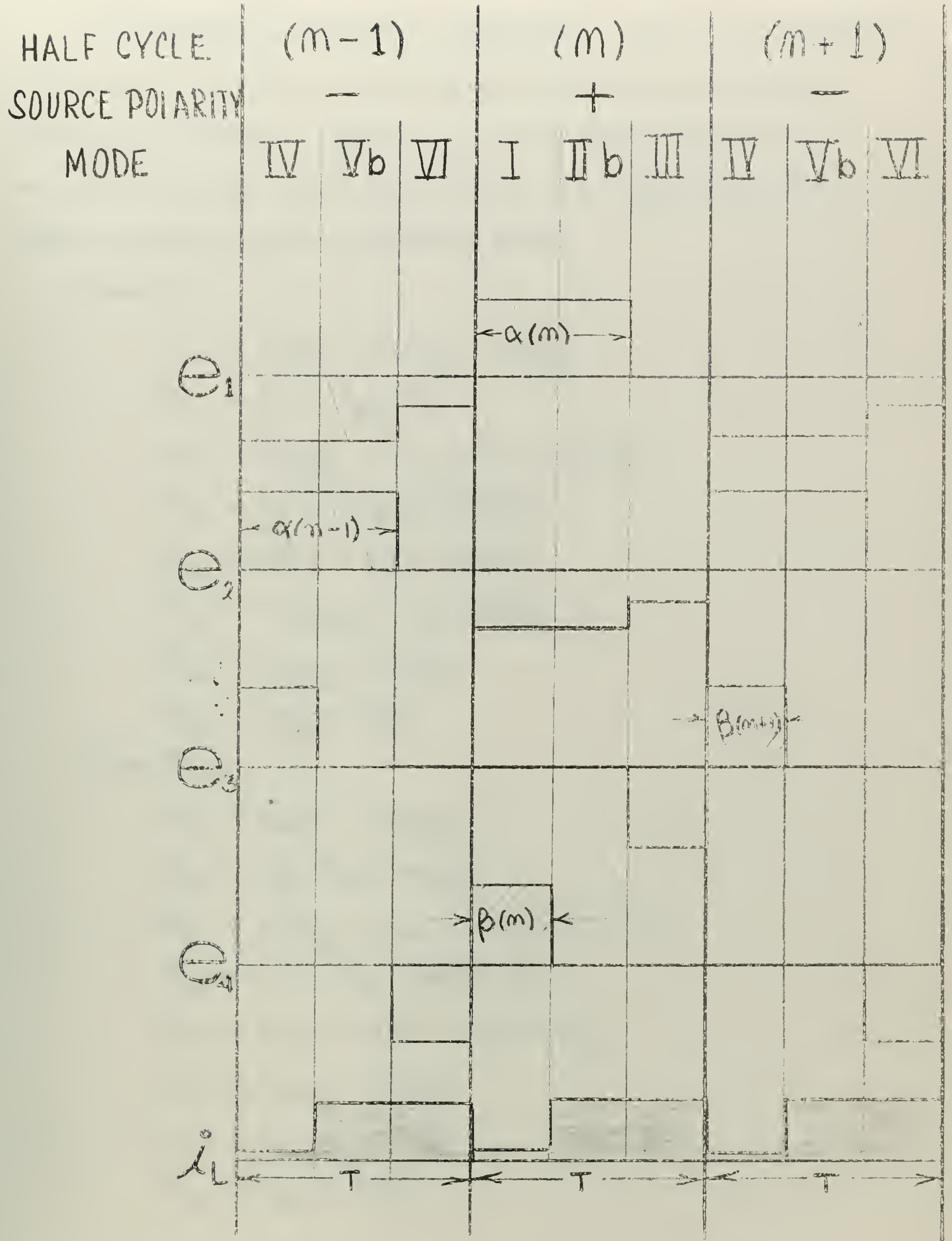
Figure 16 - Assumed Modes of Operation - Hybrid IV





HYBRID IV ASSUMED WAVEFORMS $E_c = \frac{E_{c\,MAX}}{3}$

FIGURE 17



HYBRID IV ASSUMED WAVEFORMS $E_c = \frac{2}{3} E_{c\,max}$

FIGURE 18

[illegible]

[illegible]

3. Statement of Modal Equations. Using the preceding section as a guide, the equations for each mode were written as follows. Since E_{s1} in a given half cycle has the polarity which E_{s2} has in the following half cycle, polarities are inserted here:

Mode I:

$$
\begin{aligned}
E_c &= i_c R_c - e_1/N_A - e_2/N_A \\
E_{s1} &= e_1 + i_{R1} R_A \\
E_{s1} &= e_4/N_B + V_{b2} - e_2 + i_{R1} R_5 \\
E_{s2} &= e_4 + i_{L4} (R_4+R_6+R_L) \\
E_{s2} &= 2V_{b3} + i_{L4} (R_6-R_L) \\
I_{oA} &= -i_c/N_A + i_{R1} - G_A e_1 \\
I_{oA} &= i_c/N_A + G_A e_2 \\
I_{oB} &= i_{L4} - G_B e_4
\end{aligned}
$$

Mode II a:

$$
\begin{aligned}
E_c &= i_c R_c - e_2/N_A \\
E_{s1} &= i_{R1} R_A - e_3/N_B \\
E_{s1} &= e_4/N_B + V_{b2} - e_2 + i_{R1} R_5 \\
E_{s2} &= e_4 + i_{L4} (R_4+R_6+R_L) \\
E_{s2} &= 2V_{b3} - e_3 + i_{L4} (R_6-R_L) \\
I_{oA} &= i_c/N_A + G_A e_2 \\
I_{oB} &= i_{R1}/N_B + G_B e_3 \\
I_{oB} &= i_{L4} - G_B e_4
\end{aligned}
$$

Mode II b:

$$E_c = i_c R_c - e_1/N_A - e_2/N_A$$

$$E_{s1} = e_1 + i_{R1} R_A$$

$$E_{s1} = V_{b2} - e_2 + i_{R1} R_5 \qquad E_{s2} = 2V_{b3} + i_{L4}(R_6 - R_L)$$

$$E_{s2} = i_{L4} (R_4 + R_6 + R_L)$$

$$I_{oA} = i_c/N_A + i_{R1} - G_A e_1$$

$$I_{oA} = i_c/N_A + G_A e_2$$

Mode III:

$$E_c = i_c R_c - e_2/N_A$$

$$E_{s1} = i_{R1} R_A - e_3/N_B$$

$$E_{s1} = V_{b2} - e_2 + i_{R1} R_5$$

$$E_{s2} = 2V_{b3} - e_3 + i_{L4} (R_6 - R_L)$$

$$E_{s2} = i_{L4} (R_4 + R_6 + R_L)$$

$$I_{oA} = i_c/N_A + G_A e_2$$

$$I_{oB} = i_{R1}/N_B + G_B e_3$$

4. Solution of Modal Equations. The equations for each of the modes in the preceding section were solved simultaneously. The following results were obtained for core voltages and currents:

Modes I or IV

$$e_{1(I)} = \frac{E_{s1}(1+G_A R_c N_A^2) - I_{oA} R_A (2+G_A R_c N_A^2) - G_A R_A N_A E_c}{(1+2\,G_A R_A) + G_A R_c N_A^2 (1+G_A R_A)} = e_{2(IV)}$$

$$e_{2(I)} = \frac{2 I_{oA} R_A - E_{s1} + I_{oA} R_c N_A^2 (1+G_A R_A) - N_A(1+G_A R_A) E_c}{(1+2\,G_A R_A) + G_A R_c N_A^2 (1+G_A R_A)} = e_{1(IV)}$$

$$e_{4(I)} = \frac{E_{s2} - I_{oB}R_B}{1+ G_BR_B} = e_{3(IV)}$$

$$i_{R_1(I)} = \frac{(E_{s1}G_A + I_{oA})(2 + G_AR_cN_A^2) + G_AN_AE_c}{1+2G_AR_A + G_AR_cN_A^2\ (1+G_AR_A)} = i_{R_2(IV)}$$

$$i_{L4(I)} = \frac{G_BE_{s2} + I_{oB}}{1+G_BR_B} = i_{L_3(IV)}$$

Modes II(a) or V(a)

$$e_{2(IIa)} = \frac{I_{oA}R_cN_A^2 - N_AE_c}{1+G_AR_cN_A^2} = e_{1(Va)}$$

$$e_{3(IIa)} = \frac{I_{oA}R_AN_B^2 - N_BE_{s1}}{1+G_BR_AN_B^2} = e_{4(Va)}$$

$$e_{4(IIa)} = \frac{E_{s2} - I_{oB}R_B}{1+G_BR_B} = e_{3(Va)}$$

$$i_{R_1(IIa)} = \frac{E_{s1}G_BN_B^2 + N_BI_{oB}}{1+G_BR_AN_B^2} = i_{R_2(Va)}$$

$$i_{L4(IIa)} = \frac{I_{oB} + G_BE_{s2}}{1+G_BR_B} = i_{L_3(Va)}$$

Modes II(b) or V(b)

$$e_1(II)_b = \frac{E_{s1}\ (1+G_AR_cN_A^2) - I_{oA}R_A(2+G_AR_cN_A^2) - G_AR_AN_AE_c}{1+2\ G_AR_A + G_AR_cN_A^2\ (1+G_AR_A)} = e_{2(V)b}$$

$$e_2(II)_b = \frac{2I_{oA}R_A - E_{s1} + I_{oA}R_cN_A^2\ (1+G_AR_A) - N_A(1+G_AR_A)E_c}{1+2\ G_AR_A + G_AR_cN_A^2\ (1+G_AR_A)} = e_{1(V)b}$$

$$i_{R_1(II)b} = \frac{(E_{s1}G_A + I_{oA})(2+G_AR_cN_A^2) + G_AN_AE_c}{1+2\ G_AR_A + G_AR_cN_A^2\ (1+G_AR_A)} = i_{R_2(V)b}$$

$$i_{L_4}(II)_b = \frac{E_{s2}}{R_B} = i_{L_3\ (V)b}$$

Modes III or VI

$$e_{2(III)} = \frac{I_{oA}R_cN_A^2 - N_AE_c}{1+G_AR_cN_A^2} = e_{1(VI)}$$

$$e_{3(III)} = \frac{I_{oB}R_AN_B^2 - N_BE_{s1}}{1+G_BR_AN_B^2} = e_{4(VI)}$$

$$i_{R_1(III)} = \frac{E_{s1}G_BN_B^2 + N_BI_{oB}}{1+G_BR_AN_B^2} = i_{R_2(VI)}$$

$$i_{L_4(III)} = \frac{E_{s2}}{R_B} = i_{L_3(VI)}$$

It should be noted that if any given core is followed through a full cycle, it does not matter whether the a or b sequence is followed. The core will still pass through the same sequence of voltages. The only difference will be the time that each of these voltages is present. This means that regardless of whether an input core or the output core diagonally opposite to it saturates first, (Fig. 17 or 18) a single volt-second equation can be written to express the core's change of flux over a full cycle.

<u>5. Firing Times.</u> Referring to Fig. 17, the amount of reset of core 1 in the (n-1) half cycle determines the amount of gating of core 1 in the (n) half cycle. The time of saturation of core 1 in the (n) half cycle determines the amount of reset of core 3 in the (n) half cycle. The amount of reset of core 3 in the (n) half cycle determines the amount of gating of core 3 in the (n+1) half cycle. The time of saturation of core 3 in the (n+1) half cycle determines the starting time

of load current, and therefore, its average value, in the (n+1) half cycle.

The following relations between α, the firing time of the first stage cores, and β, the firing time of the second stage cores, can be shown with the aid of the waveforms of Fig. 17. When $E_c = 0$, the values of E_{s1} vs. E_{s2} and R_A vs. R_B are adjusted so that cores 3 and 4 just saturate and reset over full half cycles. Thus:

$$e_{3(III)} = -e_{3(IV)} \text{ and } e_{4(VI)} = e_{4(I)}$$

or:

$$\frac{E_{s2} - I_{oB}R_B}{1 + G_BR_B} = -\frac{I_{oB}R_AN_B^2 - N_BE_{s1}}{1 + G_BR_AN_B^2}$$

As with the Hybrid III, a convenient way to insure this is to let: $E_{s2} = N_BE_{s1}$ and $R_B = N_B^2R_A$

If this is done, when a control voltage is applied, the magnitudes of voltages on the output cores will remain equal over successive half cycles. In this case, in order to satisfy the necessary condition of equal volt second areas, the time of reset must equal the time of gating. It is therefore obvious from Fig. 17 that the time of gating of an output core (β) must equal a half cycle (T) minus the previous time of gating of the associated input core (α):

$$\beta(n+1) = T - \alpha(n) \quad \text{and} \quad \beta(n) = T - \alpha(n-1)$$

6. Derivation of the Difference Equation. The modal equation solutions show that $i_{L(IV)} = i_{L(Va)}$.

The following half cycle average output currents were obtained by summing the integrals of the various magnitudes of current over the half cycle:

$$I_{L(n+1)} = \frac{1}{T}\left[\int_{nT}^{nT+\beta(n+1)} i_{L(IV)}\,dt + \int_{nT+\beta(n+1)}^{(n+1)T} i_{L(VI)}\,dt\right]$$

$$I_{L(n+1)} = \frac{1}{T}\left[\beta(n+1)\,(i_{L(IV)} - i_{L(VI)}) + i_{L(VI)}\,T\right]$$

substituting $T - \alpha(n)$ for $\beta(n+1)$

$$I_{L(n+1)} = i_{L(IV)} + (i_{L(VI)} - i_{L(IV)})\,\alpha(n)/T$$

therefore: $$\frac{\alpha(n)}{T} = \frac{I_{L(n+1)} - i_{L(IV)}}{i_{L(VI)} - i_{L(IV)}}$$

In the same manner it can be shown that:

$$\frac{\alpha(n-1)}{T} = \frac{I_{L(n)} - i_{L(I)}}{i_{L(III)} - i_{L(I)}}$$

The volt second equation for an input core was written over the (n − 1) and (n) half cycles:

$$\int_{(n-2)T}^{(n-2)T+\alpha(n-1)} \frac{e_{1(IV)}}{n_g A}\,dt + \int_{(n-2)T+\alpha(n-1)}^{(n-1)T} \frac{e_{1(Va)}}{n_g A}\,dt + \int_{(n-1)T}^{(n-1)T+\alpha(n)} \frac{e_{1(I)}}{n_g A}\,dt = 0$$

or: $$\left[e_{1(IV)} - e_{1(Va)}\right]\frac{\alpha(n-1)}{T} + e_{1(Va)} + e_{1(I)}\frac{\alpha(n)}{T} = 0$$

Substituting the appropriate core voltage and firing time solutions into the above resulted in a difference equation of the following form:

$$I_{L(n+1)} = \frac{K_1 + K_2 E_{c(n-1)} + I_{L(n)} \left[K_3 - K_4 E_{c(n-1)} \right] + K_5 E_{c(n)}}{K_6 + K_7 E_{c(n)}}$$

where:

$$K_1 = I_{oB}(1+G_A R_c N_A{}^2)\left[E_{s1} G_A R_c N_A{}^2 + I_{oA} R_c N_A{}^2\right]$$
$$+ G_B E_{s2}(G_A R_c N_A{}^2)\left[E_1(1+G_A R_c N_A{}^2) - I_{oA} R_A(2+G_A R_c N_A{}^2)\right]$$
$$- \frac{E_2}{R_B}\left[1+2G_A R_A + G_A R_c N_A{}^2(1+G_A R_A)\right] I_{oA} R_c N_A{}^2$$

$$K_2 = N_A \left[G_A R_A E_{s2}\left(\frac{1}{R_B} + G_B\right) + \left(\frac{E_2}{R_B} - I_{oB}\right)(1+G_A R_A)(1+G_A R_c N_A{}^2)\right]$$

$$K_3 = (1+G_B R_B)\left[E_1(1+G_A R_c N_A{}^2) - I_{oA} R_A(1+G_A R_c N_A{}^2)\right]$$

$$K_4 = (1+G_B R_B)\, G_A R_A N_A$$

$$K_5 = (I_B + G_B E_2)(1+G_A R_c N_A{}^2)\, G_A R_A N_A$$

$$K_6 = (1+G_B R_B)(1+G_A R_c N_A{}^2)\left[E_1(1+G_A R_c N_A{}^2) - I_{oA} R_A(2+G_A R_c N_A{}^2)\right]$$

$$K_7 = (1+G_B R_B)(1+G_A R_c N_A{}^2)\, G_A R_A N_A$$

From the form of this difference equation, it can be seen that this amplifier is not of the fast response type. The load current in a given half cycle depends, according to the equation, not only on input voltage in two previous half cycles, but also on the load current in the prior half cycle. Therefore, a step change in input will result in an exponential change in output, which will take a finite time greater than two half cycles, to reach steady state. This verifies the assumed method of operation, as described in the first section.

7. Verification of Analysis and Conclusion. The circuit shown in Fig. 15 was set up and operated such that full reset and gate of the second stage cores could just be achieved in full reset or gate half cycles respectively. The following parameters were measured for use in the difference equation. Diode drops, source resistances, and winding resistances have been included in these parameters:

Run #1

$R_A = 326\ \Omega$ $E_{s1} = 9.5$v. $I_{oA} = .35\text{x}10^{-3}$

$R_B = 1308\ \Omega$ $E_{s2} = 24.0$v. $G_A = .868\text{x}10^{-4}$

$R_c = 305\ \Omega$

$R_L = 1280\ \Omega$ $I_{oB} = 1.065\text{x}10^{-3}$

$n_{gA} = 450$ T. $n_{gB} = 1000$ T. $G_B = .763\text{x}10^{-4}$

$n_{cA} = 90$ T. $n_{cB} = 125$ T.

$N_A = 5$ $N_B = 8$

The solutions for the difference equation constants using the above parameters were:

$K_1 = -48.7 \times 10^{-3}$ $K_4 = .155$ $K_7 = .274$

$K_2 = 159.0 \times 10^{-3}$ $K_5 = .723 \times 10^{-3}$

$K_3 = 18$ $K_6 = 31.8$

Rearrangement of the Difference Equation for steady state operation ($I_{L(n+1)} = I_{L(n)}$) gives:

$$I_L = \frac{K_1 + (K_2 + K_5)E_c}{K_6 - K_3 + (K_7 + K_4)E_c}$$

Substituting the constant values for run #1:

$$I_L = \frac{-48.7 \times 10^{-3} + 159.7 \times 10^{-3}\ E_c}{13.8 + .429\ E_c}$$

The experimental and analytically determined results were plotted together on Fig. 19. As can be seen from the figure, the characteristics are in very serious disagreement. The volt second areas of successive reset and gate half cycles of the second stage cores were found to be in very close agreement for $E_c = 0$. That is, substituting the parameter values of run #1 in the solution for e_3 (I) and e_3 (IV), it was found that:

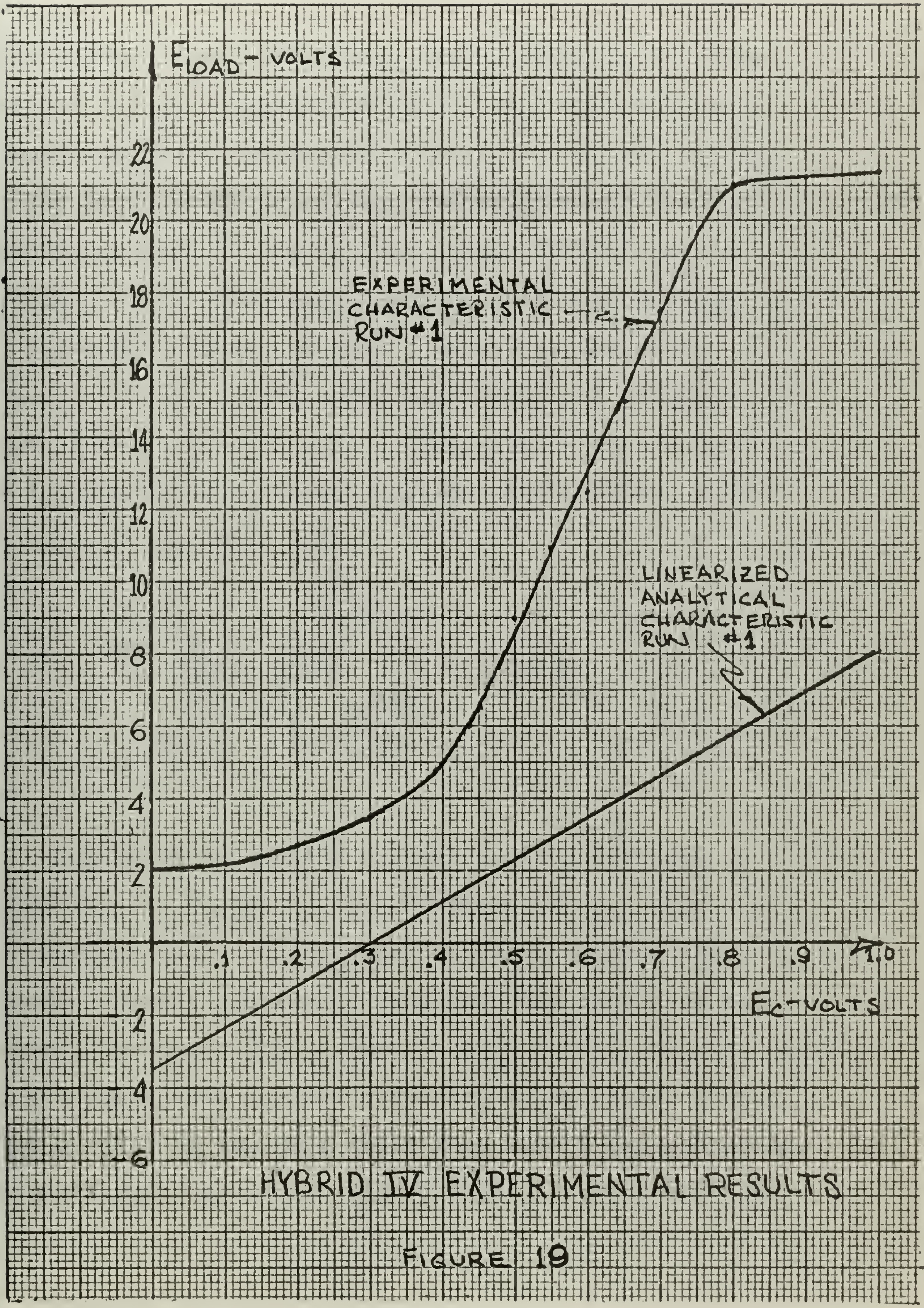
$$e_3\ (I)^T = 20.8T \text{ volt seconds}$$
$$e_3\ (IV)^T = 20.6T \text{ volt seconds}$$

and as previously stated, this was a criterion used in the analysis. Also, during that period of the half cycle when the first cores were gating, i_r was much less than the threshold magnetizing current of the second stage cores, thus satisfying another of the initial assumptions:

$$i_{r1}\ ,\ (\text{for } E_c = 1.0 \text{ volts}) = 2.051 \times 10^{-3} \text{ amps.}$$

Referred to the gate winding of the second stage cores, this current is $2.051 \times 10^{-3}/8 = .25 \times 10^{-3}$ amps, which is less than $I_{OB} = 1.065 \times 10^{-3}$ amps.

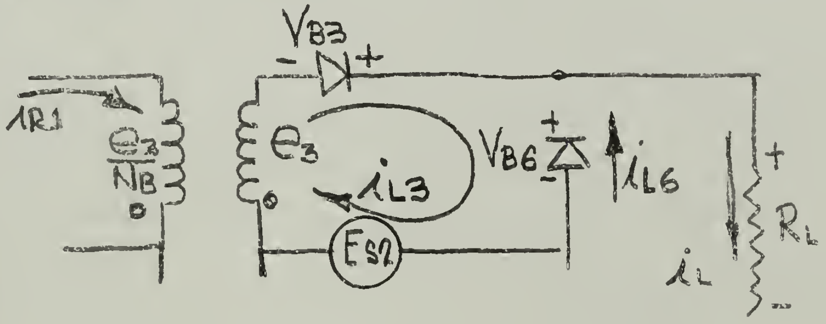
At this juncture, all of the assumptions appeared to be valid with the exception of the assumption that the diodes associated with a particular core remained blocked during those half cycles when the core was resetting.



HYBRID IV EXPERIMENTAL RESULTS

FIGURE 19

Current and voltage waveforms of the circuit used in run #1 were then studied, and it was determined that considerable diode unblocking was occuring in the load circuit diodes during those half cycles when they were assumed blocked. Referring to Fig. 20, 21, 22, and 23, it can be seen the i_{L3} flowed whenever core 3 was resetting, thus V_3 was unblocked when it was assumed blocked. This unblocking resulted from the coupling of the reset voltage of core 3 across to the gate winding of core 3 with such a magnitude and polarity that it acted to unblock V_3. The path of this current is through diode V_6 in the reverse direction and back to core 3. See Fig. below.



The negative current through V_6 is determined by examining the change in the waveforms of i_{L6}. When the circuit was opened at V_4, i_{L6} increased because the reverse current had ceased to flow. The effect of this reverse current could be clearly seen in Fig. 20, 21, and 22 by observing that i_{L6} was decreased in magnitude during that portion of the half cycle when core 3 was resetting. This circulating current flowed in a direction which

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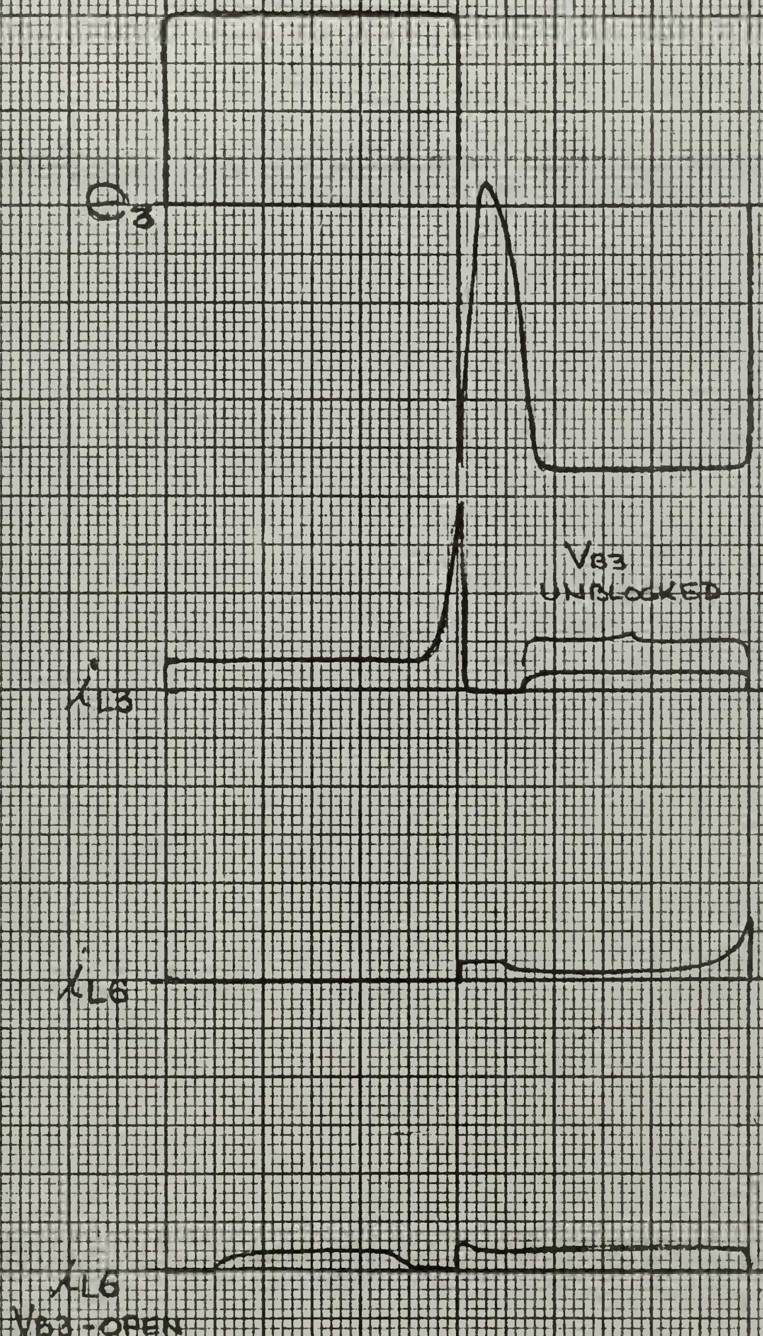
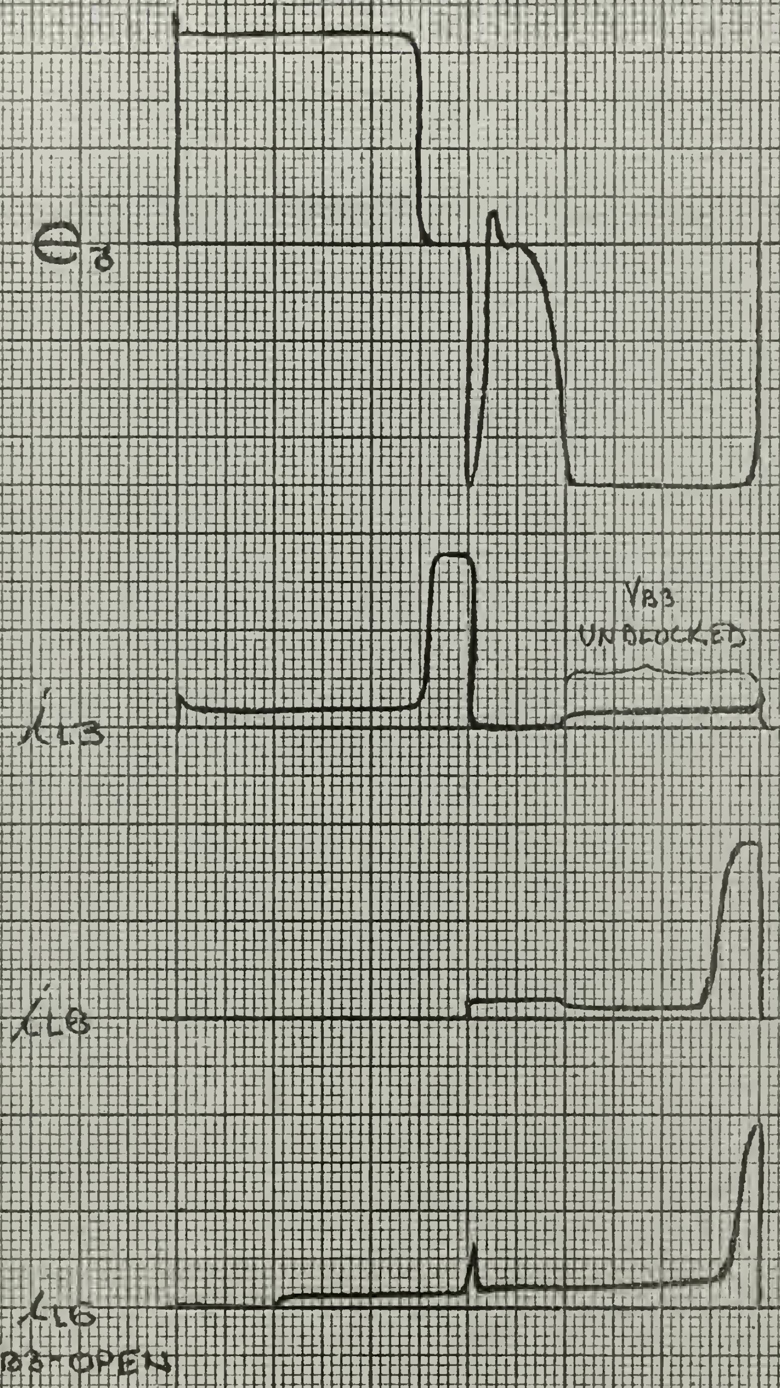
$$[illegible]$$

[illegible]



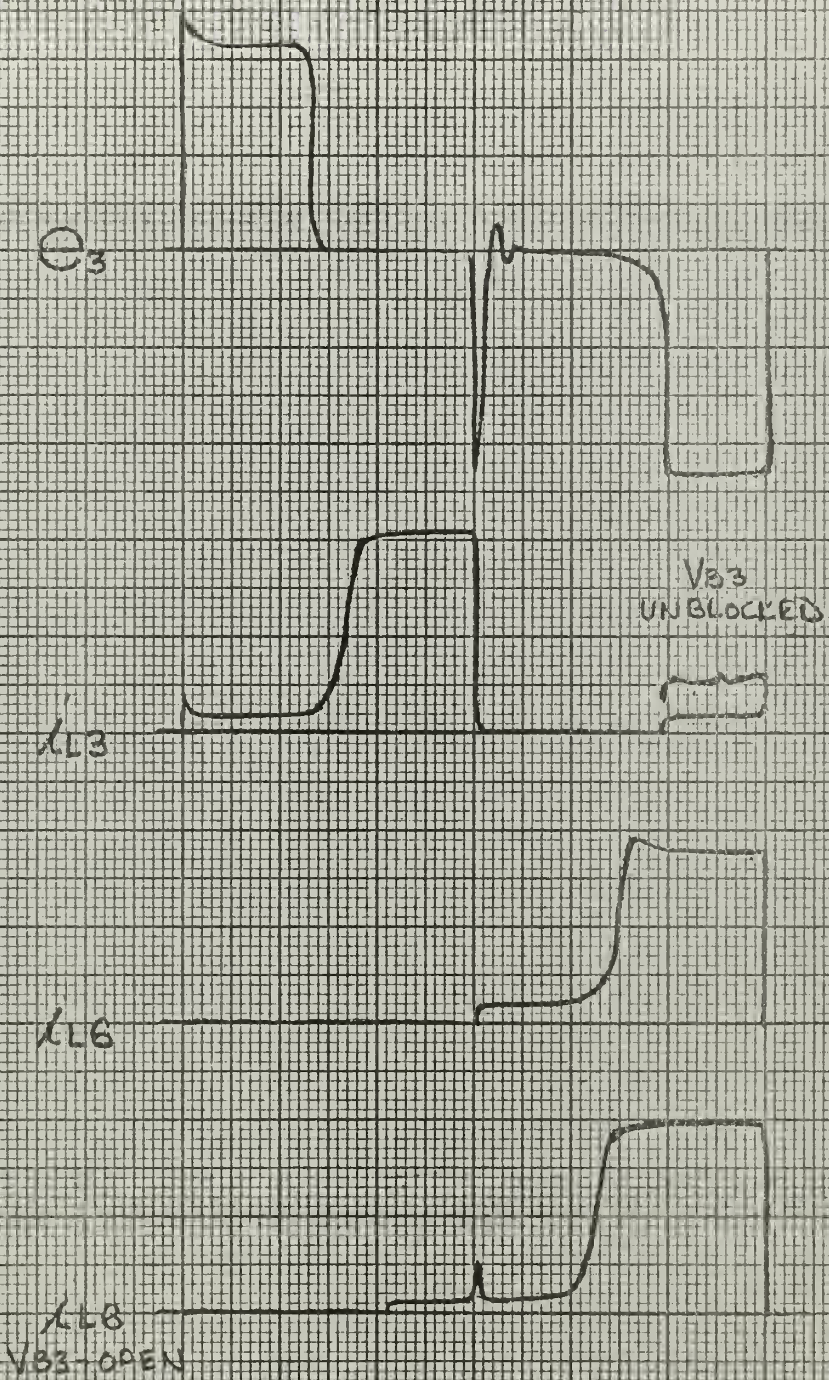
HYBRID IV WAVEFORMS SHOWING DIODE UNBLOCKING - $E_c = 0$

FIGURE 20



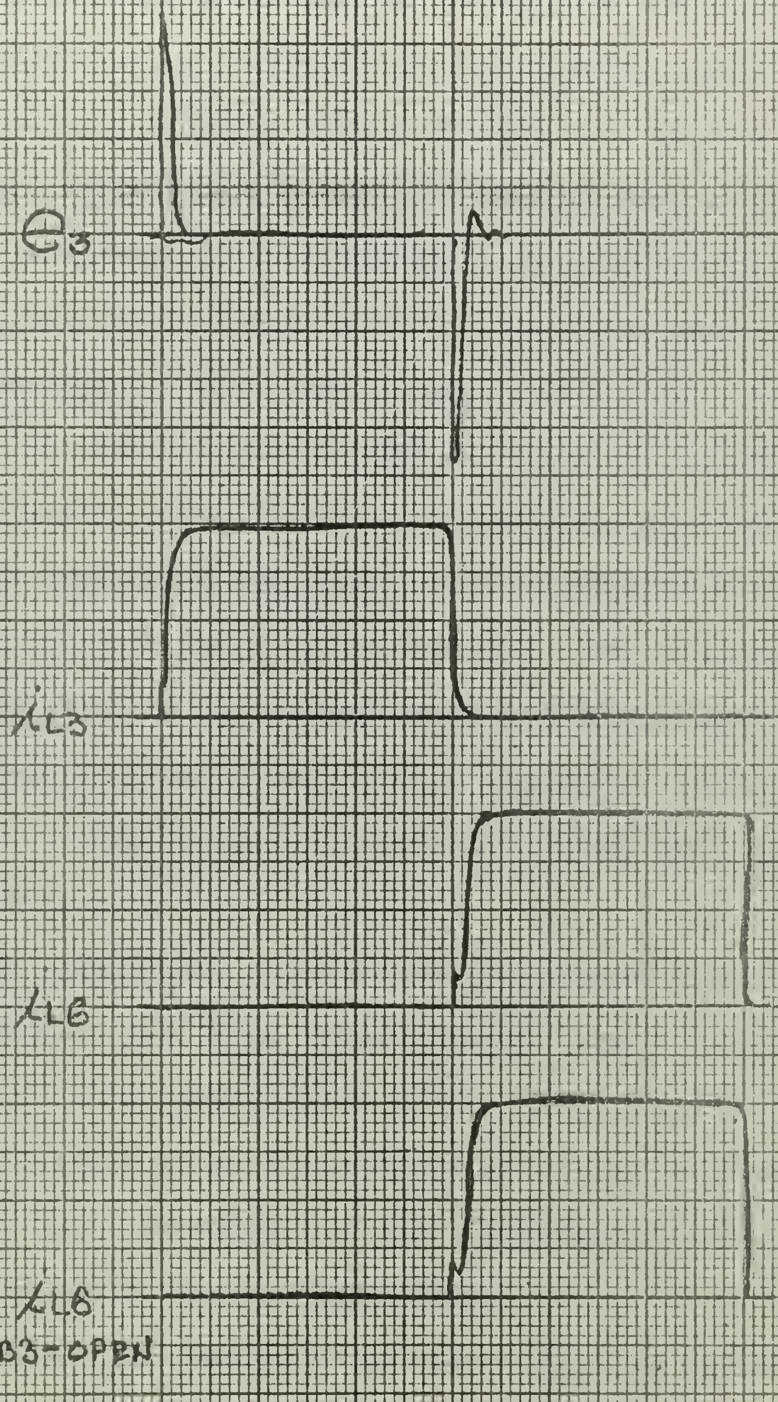
HYBRID IV WAVEFORMS SHOWING
DIODE UNBLOCKING - Ec = .4 volts

FIGURE 21



HYBRID IV WAVEFORMS SHOWING DIODE UNBLOCKING — Ec = .6 VOLTS

FIGURE 22



HYBRID IV WAVEFORMS SHOWING DIODE UNBLOCKING - E_c = .8 volts

FIGURE 23

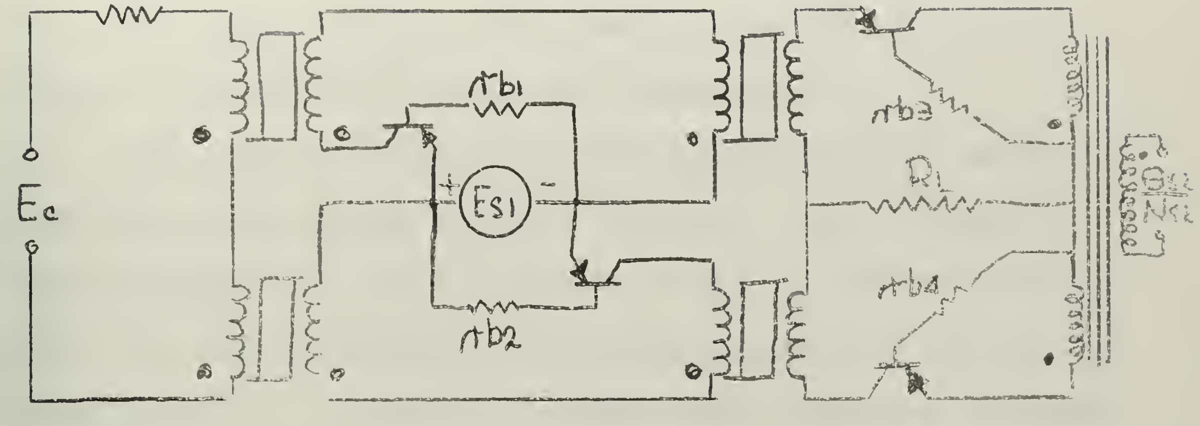
effectively was acting to gate core 3 while i_{R1} was resetting core 3. Thus, for a given output a greater amount of volt-second reset had to be applied to core 3 because the circulating currents in the load circuit were acting to hold off the reset of core 3. To get this increased volt-second reset of core 3, core 1 had to saturate sooner in its gating half cycle. This meant that E_c had to be less so core 1 would saturate sooner. Effectively, therefore, the coupling into the load circuit and the resultant unblocking of V_3 and V_4, during the reset of cores 3 and 4, acted as a positive feedback which increased the gain since a smaller amount of input was required for a given output. This unblocking resulted in an invalid difference equation since one of the major assumptions made in writing the modal equations called for all diodes to be blocked for a full half cycle out of every cycle.

The modal equations, volt-second equations, and difference equation had been checked many times before discovering the diode unblocking in the load circuit. This repeated check of the derivation was felt necessary because of the cumbersomeness of the difference equation before it was reduced to the final form.

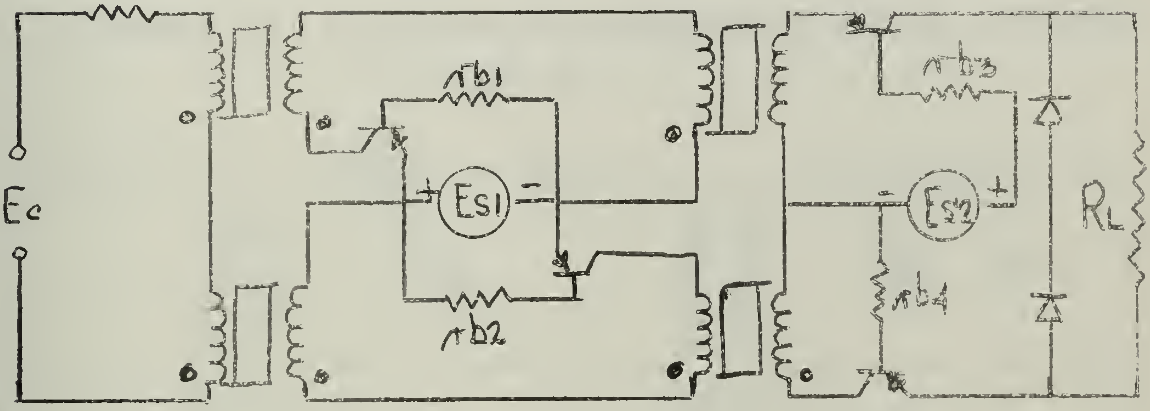
To prove that the analysis as made would be valid for a Hybrid IV circuit, operating in accordance with the initial assumptions, the following circuits were tested in an effort to eliminate any unblocking of the

diodes when they were assumed blocked.

(1) Switching Transistors in lieu of Diodes. Center-tap source for E_{s2} - Fig. 24.



(2) Switching Transistors in lieu of Diodes V_1, V_2, V_3, and V_4 - Fig. 25.



In Fig. 24 and 25, SP - 147 PNP transistors were used to switch gating current on and off in the various loops. However, even though the base resistances were varied to obtain the best switching possible, simulation of the Hybrid IV was not satisfactory because of dissimilar characteristics of the transistors and an

[illegible]

[illegible]

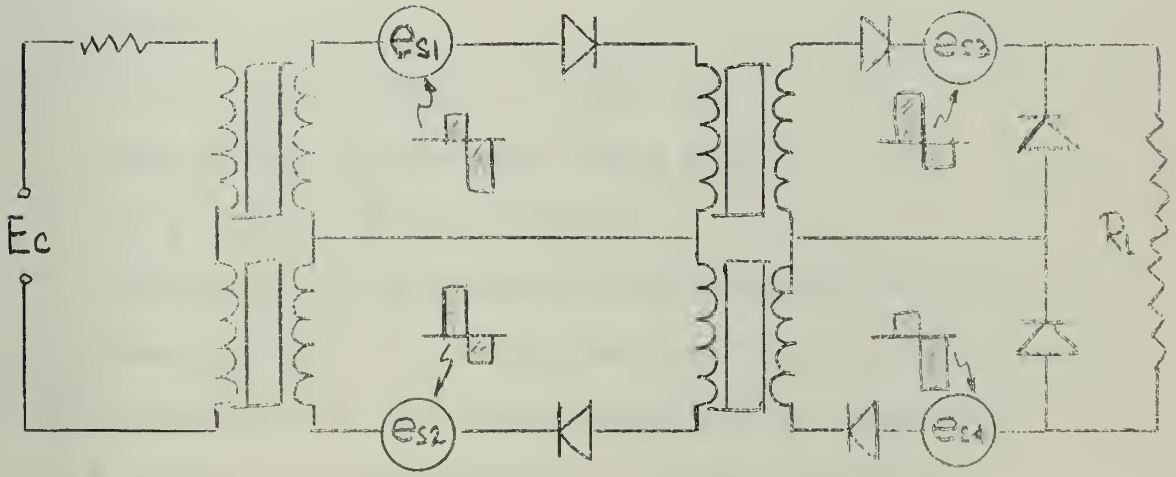
[illegible]

apparent phase lag of from 1/8 to 1/4 cycle when switching. This phase lag was evident with both sinusoidal and square wave source voltages (400 cps.). Even with the phase lag, attempts were made to achieve balanced circuit operation but were not successful.

Fig. 26 is a diagram of the circuit used to achieve the half cycle diode blocking desired. E_{s1} and E_{s2} in this diagram were used in place of E_{s1} in the circuit of Fig. 15, and E_{s3} and E_{s4} were used in place of E_{s2} in the same circuit. In order to obtain large blocking voltages during appropriate half cycles the non-symmetrical voltage circuit described in section 7 and Fig. 8 was used. Otherwise the circuits of Fig. 15 and 26 are the same.

Hybrid IV - Utilizing non-symmetrical source voltages.

Fig. 26



Run #2 was made using the circuit of Fig. 26. The experimental and difference equation characteristics have been plotted in Fig. 27.

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

The circuit parameters for run #2 were as follows:

$R_A = 144\ \Omega$ $E_{s1} = 5.36\text{v.}$ $I_{oA} = .175\times10^{-3}$

$R_B = 1388\ \Omega$ $E_{s2} = 15.90\text{v.}$ $G_A = .0216\times10^{-3}$

$R_c = 1500\ \Omega$ $I_{oB} = 1.065\times10^{-3}$

$R_L = 1280\ \Omega$ $G_B = .0763\times10^{-3}$

$n_{gA} = 900\ \text{T}$ $n_{gB} = 1000\ \text{T}$

$n_{cA} = 90\ \text{T}$ $n_{cB} = 125\ \text{T}$

$N_A = 10$ $N_B = 8$

Difference equation constants:

$K_1 = -1.331$ $K_4 = .0345$ $K_7 = .147$

$K_2 = 0.484$ $K_5 = .303\times10^{-3}$

$K_3 = 25.1$ $K_6 = 107.0$

This resulted in a steady state difference equation as follows:

$$I_L = \frac{-1.331 + (.428 + .303\times10^{-3})\ E_c}{81.9 + .1815\ E_c}$$

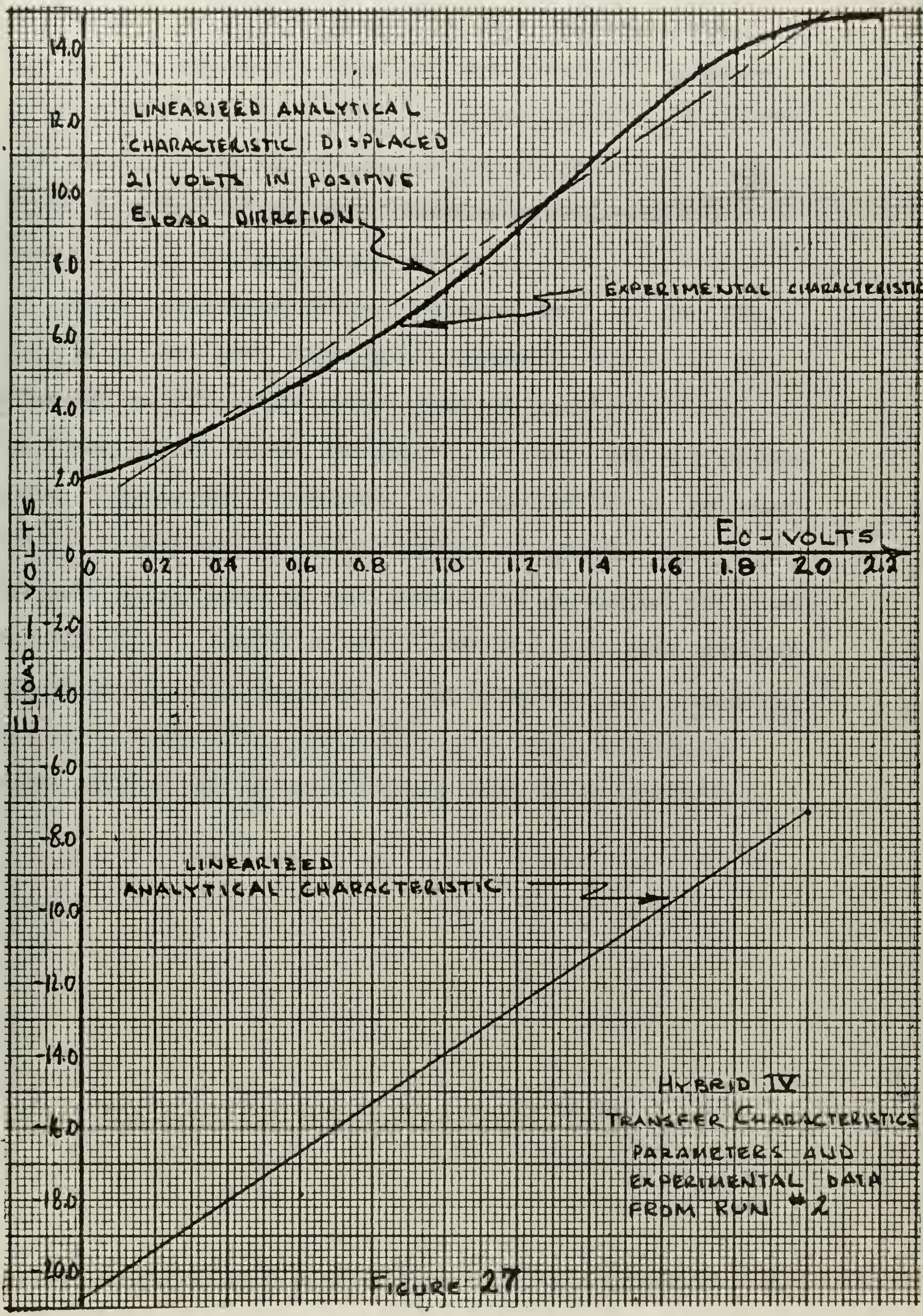
or:

$$I_L \approx -.01625 + .00534\ E_c$$

For an R_L of 1280 ohms, this gave:

$$E_L \approx -20.8 + 6.83\ E_c$$

The plot of the analytical solution of run #2 is shown in Fig. 27. This plot shows the characteristic to be entirely in the fourth quadrant for the range of E_c used in the experiment. If the linearized analytical transfer characteristic is displaced 21.8 volts in the positive E_L direction its slope, and therefore the gain, corresponds fairly well with that of the experimental characteristic. The fact that the analytical



HYBRID IV
TRANSFER CHARACTERISTICS
PARAMETERS AND
EXPERIMENTAL DATA
FROM RUN #2

FIGURE 27

solution lies entirely in the fourth quadrant is not explained. It would appear that the constant term, K_1, in the difference equation was in error. However, even though this is the most complex term, the solution had been checked and rechecked and it is believed that there were no errors made in the derivation of the terms of the difference equation.

This investigation has revealed that the two stage amplifier does have high gain. However, the diode unblocking in the final stage resulted in a positive feedback effect which, though it accounts for the higher gain, considerably increases the complexity of the modes. Future investigation of the Hybrid IV circuit should include the effects of the unblocking described previously and attempt to derive a valid equation that will describe the transfer characteristic. An investigation comparing two stage amplifier performance with that of single stage amplifiers in series would also be of interest.

APPENDIX A

DETERMINATION OF CORE PARAMETERS

If a way could be found to obtain a curve which related the magnetomotive force (mmf) applied to a core during the time flux change was taking place, to the volts per turn on the core during the same period, as in Fig. 19, it should be possible to find the constants in the expression:

$$F = n\, I_o + n\, G\, e$$

as follows:

Let n = no. of gating turns
k = slope of the mmf vs. volts/turn curve
F = total mmf
F_o = magnetizing mmf (before flux change)
I_o = magnetizing current
G = dynamic core conductance

Then, from Fig. 28:

$$F = F_o + \frac{1}{K} \times \frac{e}{n}$$

Comparing this with the core characteristic shown above:

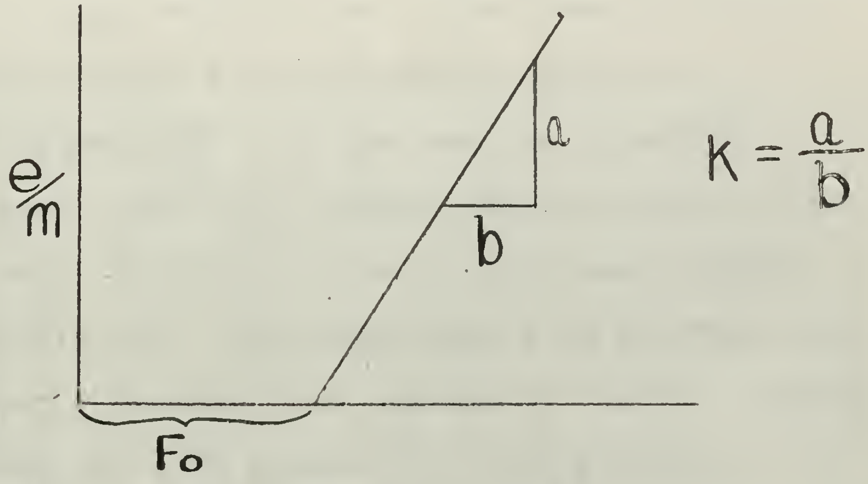
$$F_o = n\, I_o$$

$$n\, G = 1/kn$$

So: $I_o = F_o/n$

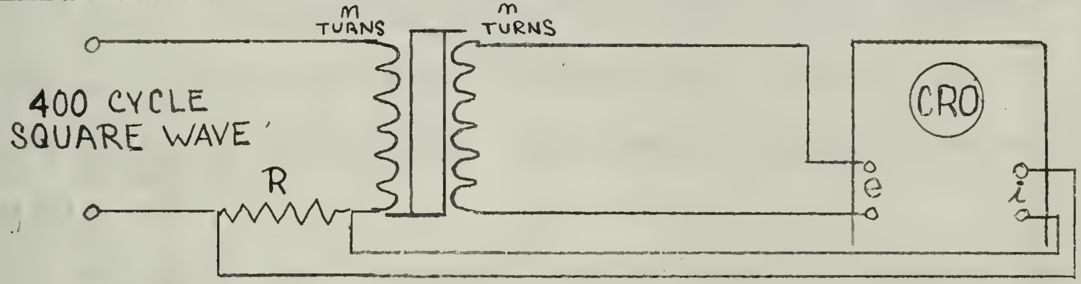
And: $G = 1/k \times 1/n^2$

This characteristic can be obtained by the circuit of Fig. 29. The voltage on the core is displayed.



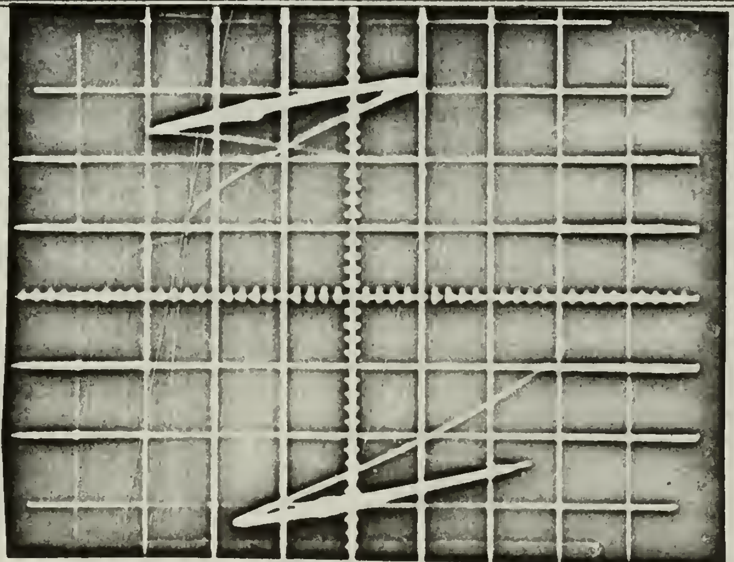
MMF VERSUS VOLTS PER TURN

FIGURE 28



CIRCUIT FOR DETERMINING MMF vs e/n CHARACTERISTIC

FIGURE 29



PHOTOGRAPH OF TYPICAL e-i CURVE

FIGURE 30

vertically on the oscilloscope, simultaneously with a voltage proportional to the current, which is displayed horizontally. As the core is alternately gated and reset, the volts versus current pattern will be traced out. The result, for a square wave input, is shown in Fig. 30. The bright spots in the Fig. are the locations of current and voltage at the core conduction in which the core spends the major portion of its time, namely, when the flux is changing. By varying the supply voltage, the amount of reset can be varied from zero up to the onset of saturation. The locus of a bright spot will then trace out the desired curve of Fig. 28.

The data from the above was adjusted to include the values of the current measuring resistance and the number of turns. The results are shown for both cores in Fig. 31. These results are expanded for each core on Fig. 32 and 33. Straight line curves were approximated by connecting the point where saturation begins to the point representing voltage for half saturation, and these lines were used to derive the core values as follows:

Core A:

Magnetics, Inc. core #50106 - 2D
material - Hy Mu 80 $n = 900$ turns
$I_o = .35 \times 10^{-3}$ amps. $G = .868 \times 10^{-4}$ mhos.

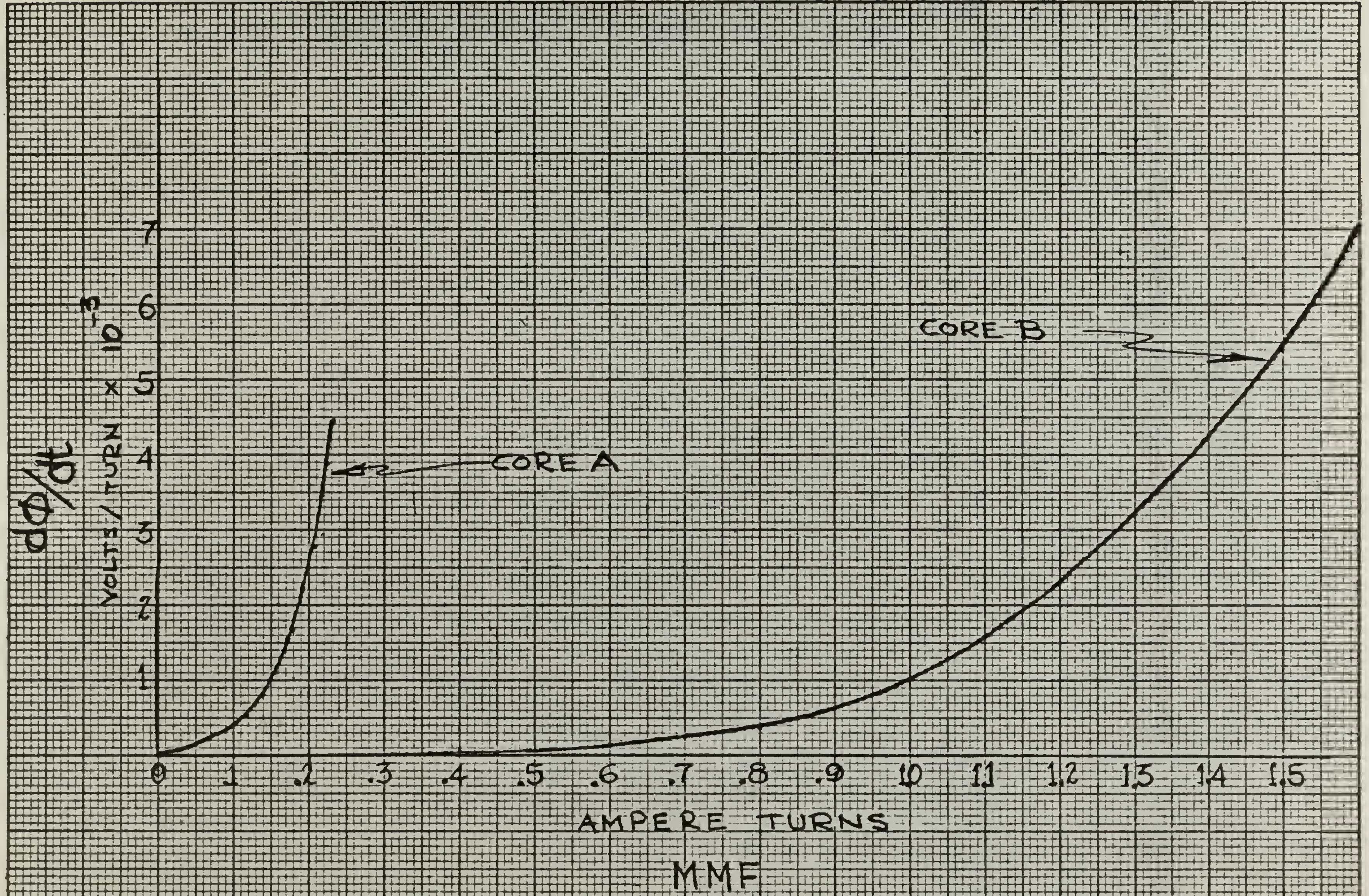
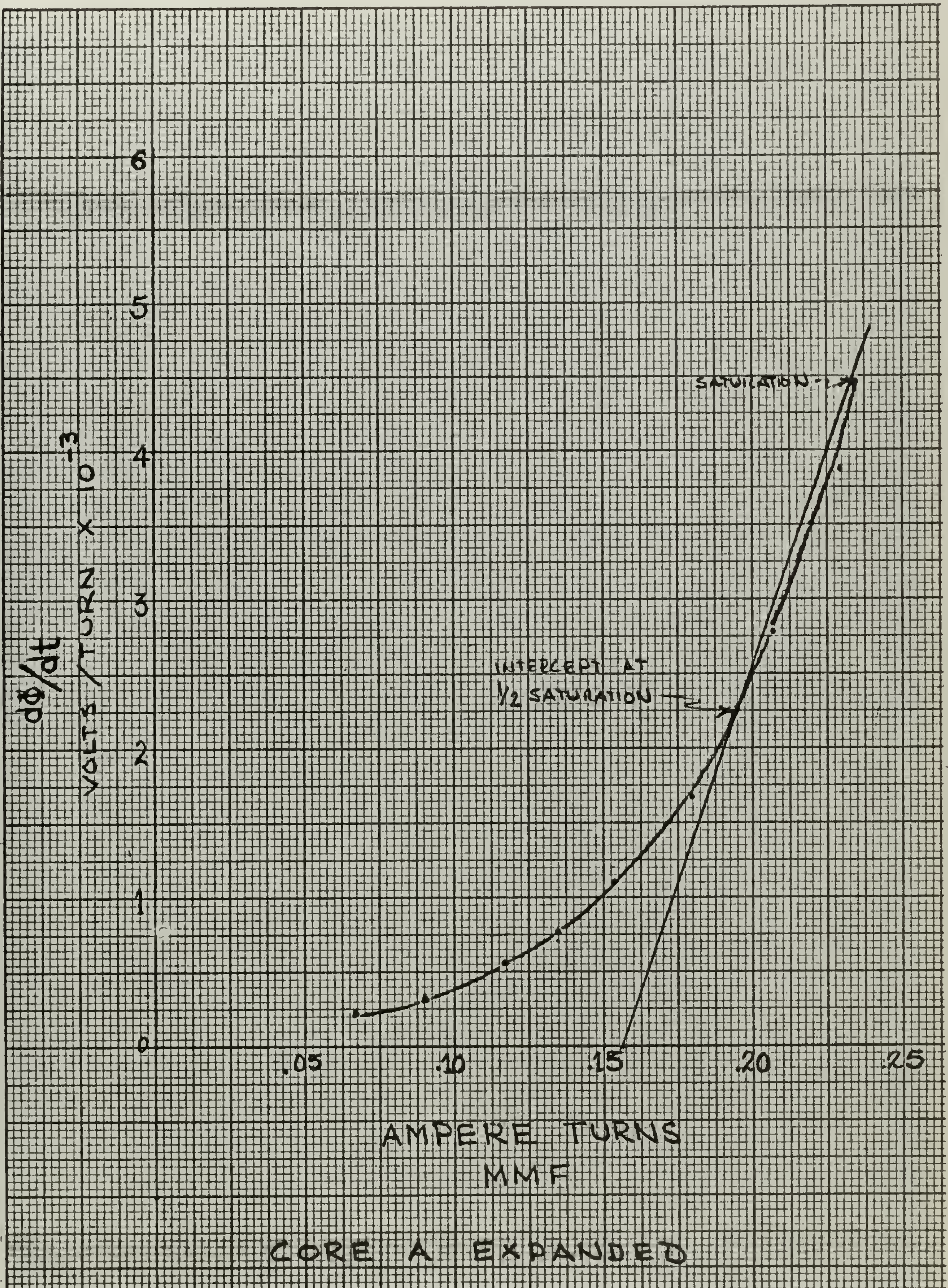
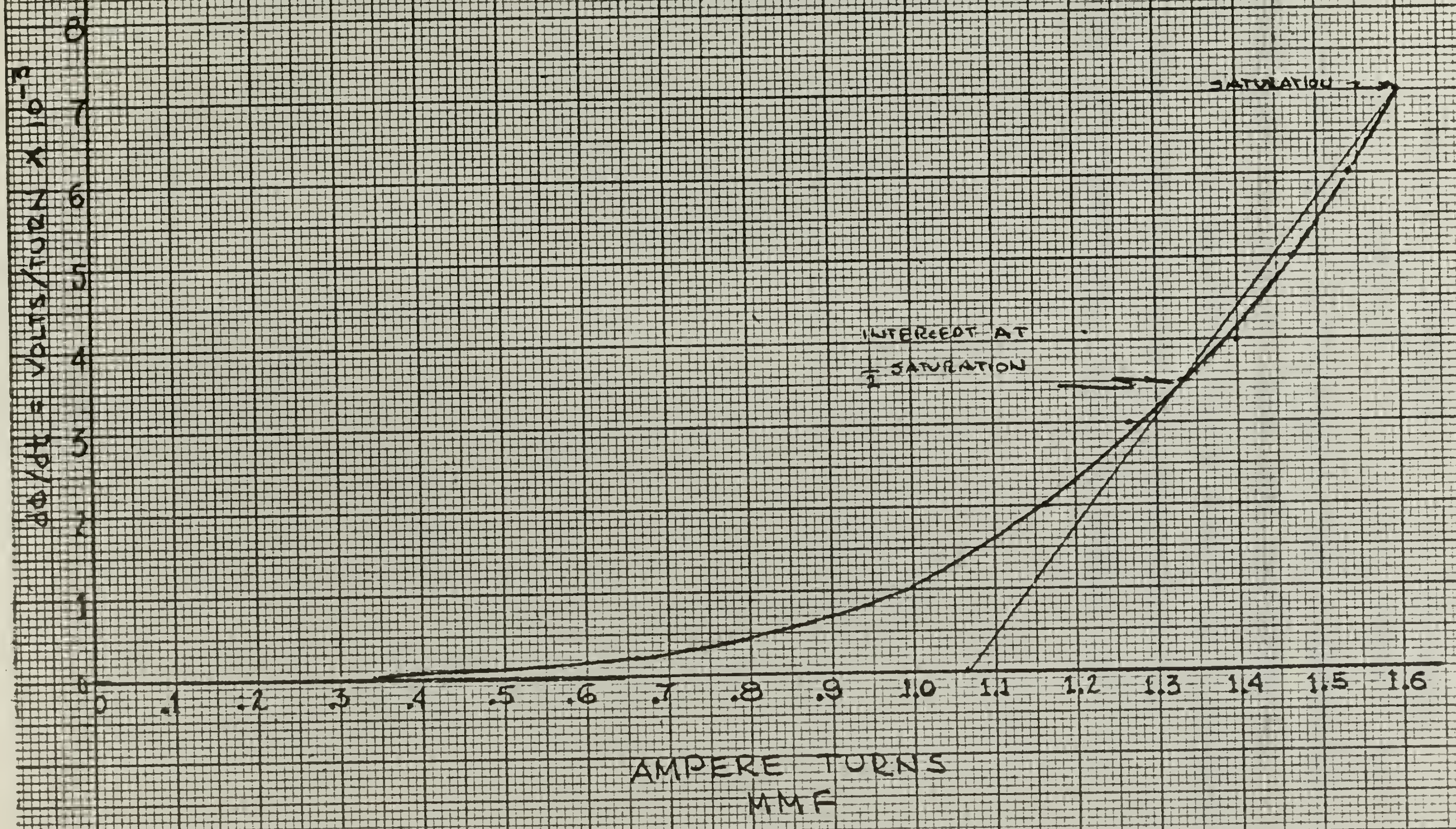

$d\Phi/dt$
VOLTS / TURN × 10^{-3}
0
1
2
3
4
5
6
7
CORE A
CORE B
0 .1 .2 .3 .4 .5 .6 .7 .8 .9 1.0 1.1 1.2 1.3 1.4 1.5
AMPERE TURNS
MMF

FIGURE 31



CORE A EXPANDED

FIGURE 32



CORE B EXPANDED

FIGURE 33

Core B:

Magnetics Inc. core #50004 - 2A

material - Orthonol $n = 1000$ turns

$I_o = 1.065 \times 10^{-3}$ $G = .763 \times 10^{-4}$ mhos.

It should be noted for core A, that although 900 turns was used to take the data, and therefore, to compute the volts per turn, the n used in the equations for I_o and G was the number of turns used in the amplifier experimentally, i.e., 450 turns.

APPENDIX B

RESULTS OF PARTIAL ANALYSIS CONSIDERING SOURCE RESISTANCE

In order that anyone wishing to continue the analysis of the Hybrid III amplifier may utilize what results have been obtained, the following partial analysis is presented.

The circuit to be analyzed is shown in Fig. 34. The assumed modes of analysis are as were shown in Fig. 11. Using these two figures the equations for each mode were written as follows:

Mode I:

$$e_c = i_c R_c - e_1/N_A$$

$$e_{s1} = e_1 + i_{R1}\,(R_A + R_{s1}) + i_{R2}\,(R_{s1})$$

$$e_{s1} = i_{R2}\,(R_A + R_{s1}) + i_{R1}\,(R_{s1}) - e_4/N_B$$

$$-e_{s2} = -V_{b3}$$

$$-e_{s2} = e_4 - V_{b4}$$

$$-i_c/N_A + i_{R1} = I_{oA} + G_A e_1$$

$$-i_{R2}/N_B = -I_{oB} + G_B e_4$$

Mode II:

$$e_c = i_c R_c$$

$$e_{s1} = i_{R1}\,(R_A + R_{s1}) + i_{R2}\,(R_{s1}) - e_3/N_B$$

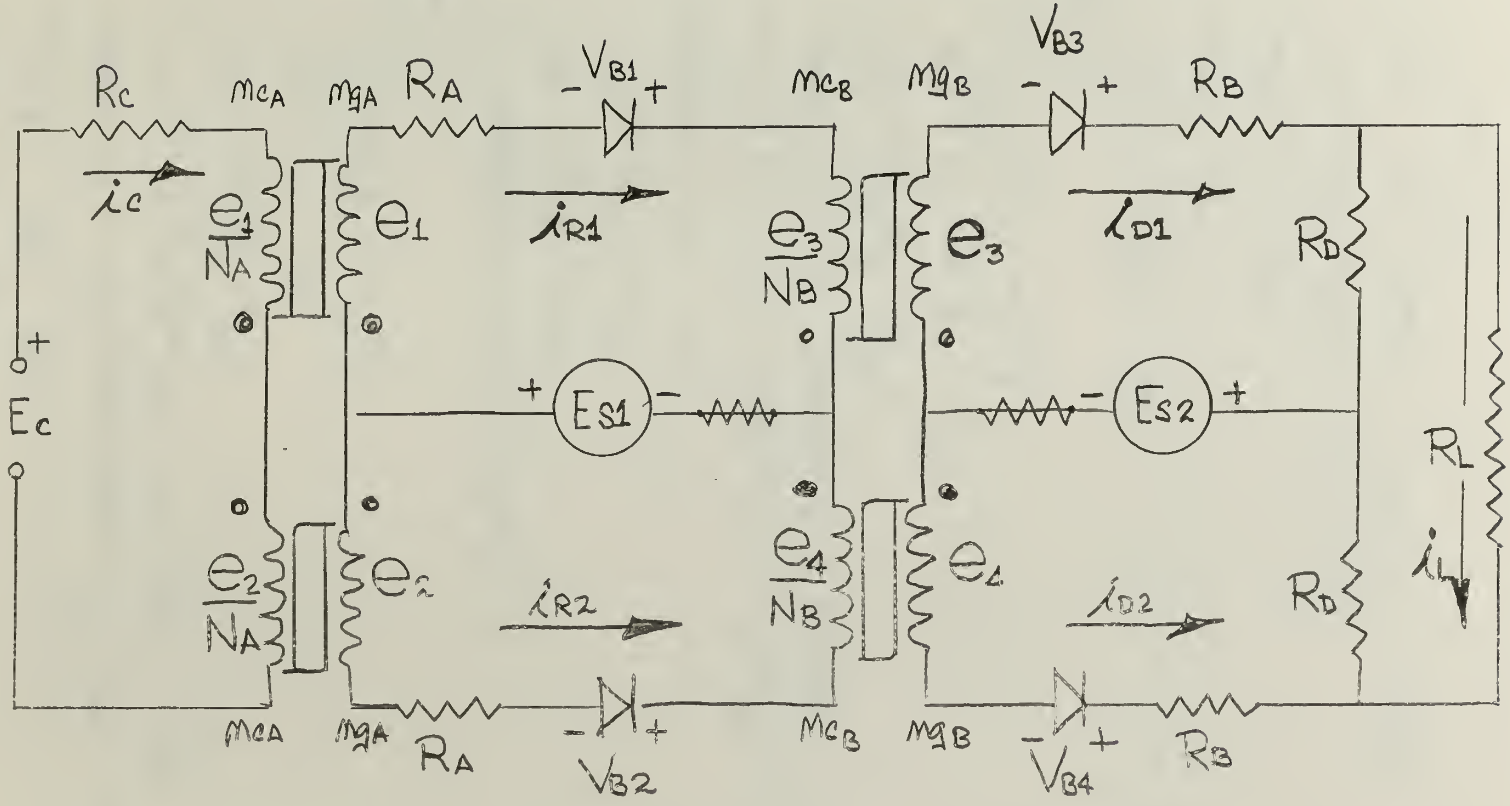
$$e_{s1} = i_{R2}\,(R_A + R_{s1}) + i_{R1}\,(R_{s1}) - e_4/N_B$$

$$-e_{s2} = e_3 - V_{b3}$$

$$-e_{s2} = e_4 - V_{b4}$$

$$-i_{R1}/N_B = -I_{oB} + G_B e_3$$

$$-i_{R2}/N_B = -I_{oB} + G_B e_4$$



THE HYBRID III MAGNETIC AMPLIFIER CIRCUIT WITH SOURCE RESISTANCE

FIGURE 34

[illegible]

Mode III:

$$e_c = i_c R_c$$

$$e_{s1} = i_{R1} (R_A+R_{s1}) + i_{R2} (R_{s1}) - e_3/N_B$$

$$e_{s1} = i_{R2} (R_A+R_{s1}) + i_{R1} (R_{s1})$$

$$-e_{s2} = e_3 - V_{b3}$$

$$-e_{s2} = -V_{b4}$$

$$-i_{R1}/N_B = -I_{oB} + G_B e_3$$

Mode IV:

$$e_c = i_c R_c - e_1/N_A$$

$$e_{s1} = e_1 - e_3/N_B - V_{b1}$$

$$e_{s1} = -e_4/N_B - V_{b2}$$

$$-e_{s2} = e_3 + i_{D1} (R_B+R_D+R_{s2}) + i_{D2}(R_{s2}) - i_L R_D$$

$$-e_{s2} = e_4 + i_{D2} (R_B+R_D+R_{s2}) + i_{D1}(R_{s2}) + i_L R_D$$

$$-i_c/N_A = -I_{oA} + G_A e_1$$

$$i_{D1} = I_{oB} + G_B e_3$$

$$i_{D2} = I_{oB} + G_B e_4$$

$$i_L (2R_D+R_L) + i_{D2} R_D - i_{D1} R_D = 0$$

Mode V:

$$e_c = i_c R_c - e_1/N_A$$

$$e_{s1} = e_1 - V_{b1}$$

$$e_{s1} = -e_4/N_B - V_{b2}$$

$$-e_{s2} = i_{D1}(R_B+R_D+R_{s2}) + i_{D2} (R_{s2}) - i_L R_D$$

$$-e_{s2} = e_4 + i_{D2} (R_B+R_D+R_{s2}) + i_{D1} (R_{s2}) + i_L R_D$$

$$-i_c/N_A = -I_{oA} + G_A e_1$$

$$i_{D2} = I_{oB} + G_B e_4$$

$$i_L (2 R_D + R_L) + i_{D2} R_D - i_{D1} R_D = 0$$

The solutions for those voltages that were solved for, with voltage polarities inserted, are as follows:

Mode I.

$$e_1 = \frac{\left[G_B\,(R_A{}^2+2R_AR_{s1}) + R_A+R_{s1}/N_B{}^2\right]\left[-\frac{E_c}{N_A} - I_{oA}\,R_c\right] + E_{s1}R_c\,(G_BR_A+\frac{1}{N_B{}^2}) - I_{oB}R_{s1}R_c/N_B}{\left[G_AR_c+\frac{1}{N_A{}^2}\right]\left[G_B\,(R_A{}^2+R_AR_{s1}) + \frac{R_A+R_{s1}}{N_B{}^2}\right] + G_BR_c(2R_A+R_{s1}) + \frac{R_c}{N_B{}^2}}$$

Mode II.

$$e_3 = \frac{\left[\frac{1}{N_B} + G_BN_BR_A\right]\left[I_{oB}R_A + 2\,I_{oB}R_{s1} - \frac{E_{s1}}{N_B}\right]}{\left[\frac{2}{N_B} + G_BN_BR_A\right]\left[G_B\,(R_A+R_{s1})\right] + \frac{1}{N_B{}^3} + G_B{}^2\,N_BR_AR_{s1}}$$

Mode III.

$$e_3 = \frac{I_{oB}\,R_A{}^2 + 2\,I_{oB}\,R_AR_{s1} - \frac{E_{s1}\,R_A}{N_B}}{G_BR_A{}^2 + 2G_BR_AR_{s1} + \frac{R_A}{N_B{}^2} + \frac{R_{s1}}{N_B{}^2}}$$

Mode IV.

$$e_1 = \frac{I_{oA} - \frac{E_c}{N_A}R_c}{G_A + \frac{1}{N_A{}^2R_c}}$$

$$e_3 = \frac{\begin{gathered}\left[I_{oB} - G_B E_{s2}\right] \left[R_D^2 - (2R_D+R_L)(R_B+R_D+R_{s2})\right] \\ + \left[2R_D+R_L\right] \left[(1-G_B R_{s2})(E_{s2}-I_{oB}R_{s2})-I_{oB}G_B(R_B+R_D+R_{s2})^2\right] \\ + (2I_{oB}G_B R_D^2) \quad (R_B+R_D+2R_{s2}) - I_{oB}R_D^2\end{gathered}}{\begin{gathered}\left[2R_D+R_L\right] \left[1+2G_B \quad (R_B+R_D+R_{s2}) + G_B^2(R_B+R_D+R_{s2})^2 - G_B^2 R_{s2}^2\right] \\ - G_B^2 \left[2 \, (R_B+R_D+2R_s)(R_D^2)\right] - 2G_B R_D^2\end{gathered}}$$

Mode V.

$$e_1 = \frac{I_{oA} - \frac{E_c}{N_A^2 R_c}}{G_A + \frac{1}{N_A^2 R_c}}$$

$$i_L = \frac{E_{s2} R_D - I_{oB}R_D (R_B+R_D+2R_{s2})}{\begin{gathered}\left[(2R_D+R_L)(R_B+R_D+R_{s2}) - 2R_D^2\right]\left[1+G_B(R_B+R_D+R_{s2})\right] \\ - G_B R_{s2} \left[(2R_D+R_L)(R_{s2}) + 2R_D^2\right] + R_D^2\end{gathered}}$$

To complete the solution, it will be necessary to solve for e_4 in all modes, and then to write volt second equations as detailed in the body of the thesis to relate input to output.

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